

LVT Logic
Low-Voltage Technology
A 5-V Tolerant, 3.3-V Line of Products

Data Book

1998

Logic Products

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The SN74LVTH1500, SN74LVTH1601, SN74LVTH1602, and SN74LVTH1603 are shown as product preview in this data book. The corresponding production data LVT data sheets for these devices are available through the TI home page at <http://www.ti.com>.

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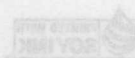
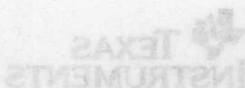
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INTRODUCTION

The 3.3-V LVT family uses the latest 0.8- μ BiCMOS process technology with performance specifications ideal for networking and telecommunication applications. In addition to popular octal and Widebus™ bus-interface devices, Texas Instruments (TI™) also offers the universal bus transceiver (UBT™) in this low-voltage family.

Performance characteristics of the LVT family are:

- **Speed** – Provides high performance with maximum propagation delays of 3.5 ns for buffers.
- **3.3-V Operation With 5-V Tolerant I/Os** – Capability to interface with a mixed-voltage environment. The I/Os can handle up to 7 V, which allows them to act as 5-V to 3-V translators.
- **High Drive/Low Power** – The LVT family provides up to 64 mA of drive, yet consumes less than 100 μ A of standby power at 3.3-V V_{CC} .

Additional features include:

- **Live Insertion** – LVT devices incorporate circuitry to protect the devices in live-insertion applications. The devices go into the high-impedance state during power up and power down [power-up 3-state (PU3S)].
- **Bus Hold** – Bus hold prevents floating inputs by holding inputs at the last valid logic state. This eliminates the need for external pullup and pulldown resistors.
- **Damping-Resistor Option** – TI implements series-damping resistors on selected devices, which reduces overshoot and undershoot and helps match the line impedance to minimize ringing.
- **Packaging** – LVT devices are available in packaging options, such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP) for octal and Widebus devices.

Some of the information in this data book is product preview. More information is available on these products, including availability dates, pricing, and final timing specifications. Please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI home page at <http://www.ti.com>.

TI also offers a complete line of low-voltage CMOS products, including Advanced Low-Voltage CMOS (ALVC), Low-Voltage CMOS (LVC), and Low-Voltage HCMOS (LV). For a complete listing of these and other TI logic solutions, please order the Logic Selection Guide (literature number SDYU001) by calling the literature response center at 1-800-477-8924.

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† The SN74LVTH1630, SN74LVTH1630T, SN74LVTH1630T, and SN74LVTH1633 are shown as product preview in this data book. The corresponding production data VLT data sheets for these devices are available through the TI home page at <http://www.ti.com>.

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

operating conditions and characteristics (in sequence by letter symbols)

C_i	Input capacitance The internal capacitance at an input of the device
C_{io}	Input/output capacitance Input-to-output internal capacitance; transcapacitance
C_o	Output capacitance The internal capacitance at an output of the device
C_{pd}	Power dissipation capacitance Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages): $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$
f_{max}	Maximum clock frequency The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification
I_{CC}	Supply current The current into* the V _{CC} supply terminal of an integrated circuit
ΔI_{CC}	Supply current change The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V _{CC}
I_{CEX}	Output high leakage current The maximum leakage current into the collector of the pulldown output transistor when the output is high and the output forcing condition V _O = 5.5 V
I_{I(hold)}	Input hold current Input current that holds the input at the previous state when the driving device goes to a high-impedance state
I_{IH}	High-level input current The current into* an input when a high-level voltage is applied to that input
I_{IL}	Low-level input current The current into* an input when a low-level voltage is applied to that input
I_{off}	Input/output power-off leakage current The maximum leakage current into/out of the input/output transistors when forcing the input/output to 4.5 V and V _{CC} = 0 V
I_{OH}	High-level output current The current into* an output with input conditions applied that, according to the product specification, establishes a high level at the output

*Current out of a terminal is given as a negative value.

GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

I_{OL}	Low-level output current The current into* an output with input conditions applied that, according to the product specification, establishes a low level at the output
I_{OZ}	Off-state (high-impedance-state) output current (of a 3-state output) <div> <div>I_{OZ}</div> <div>The current that flows through the output gates when the device is in the high-impedance state</div> </div> <div> <div>I_{OZPU}</div> <div>The current that flows into or out of the output stage when the device is being powered up from the high-impedance state</div> </div> <div> <div>I_{OZPD}</div> <div>The current that flows into or out of the output stage when the device is being powered down from the high-impedance state</div> </div>
t_a	Access time The time interval between the application of a specified input pulse and the availability of valid signals at an output
t_c	Clock cycle time Clock cycle time is $1/f_{\max}$.
t_{dis}	Disable time (of a 3-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state NOTE: For 3-state outputs, $t_{dis} = t_{PHZ}$ or t_{PLZ} . Open-collector outputs change only if they are low at the time of disabling, so $t_{dis} = t_{PLH}$.
t_{en}	Enable time (of a 3-state or open-collector output) The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low) NOTE: In the case of memories, this is the access time from an enable input (e.g., \overline{OE}). For 3-state outputs, $t_{en} = t_{PZH}$ or t_{PZL} . Open-collector outputs change only if they are responding to data that would cause the output to go low, so $t_{en} = t_{PHL}$.
t_h	Hold time The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.
t_{pd}	Propagation delay time The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH})
t_{PHL}	Propagation delay time, high-to-low level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

*Current out of a terminal is given as a negative value.



GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS



t_{PHZ}	Disable time (of a 3-state output) from high level The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state
t_{PLH}	Propagation delay time, low-to-high level output The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level
t_{PLZ}	Disable time (of a 3-state output) from low level The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state
t_{PZH}	Enable time (of a 3-state output) to high level The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level
t_{PZL}	Enable time (of a 3-state output) to low level The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level
t_{sk(o)}	Output skew The difference between any two propagation delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching output. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.
t_{su}	Setup time The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected. 2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.
t_w	Pulse duration (width) The time interval between specified reference points on the leading and trailing edges of the pulse waveform
Δt/Δv	Input voltage transition rate The input transition rise or fall rate corresponding to the change in signal amplitude with time
Δt/ΔV_{CC}	Power supply power-up rate The power-up ramp rate corresponds to the transition rate of the supply voltage when the device is being powered up.
V_{IH}	High-level input voltage An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS



V_{IL}	Low-level input voltage An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.
V_{OH}	High-level output voltage The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output
V_{OL}	Low-level output voltage The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output
V_{IT+}	Positive-going input threshold level The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V _{IT-}
V_{IT-}	Negative-going input threshold level The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V _{IT+}

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a . . . h	=	the level of steady-state inputs A through H, respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
\bar{Q}_0	=	complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
	=	one high-level pulse
	=	one low-level pulse
Toggle	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid when the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid when the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0 , or \bar{Q}_0), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction of those shown have no effect at the output. (If the output is shown as a pulse,  or , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

EXPLANATION OF FUNCTION TABLES

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

FUNCTION TABLE													
INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	H	H	H	H	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	L	L	L	L	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low, regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that as long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Because on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, regardless of the serial input, the data entered at A is at output Q_A, data entered at B is at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D, respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

The function-table functional tests do not reflect all possible combinations or sequential modes.

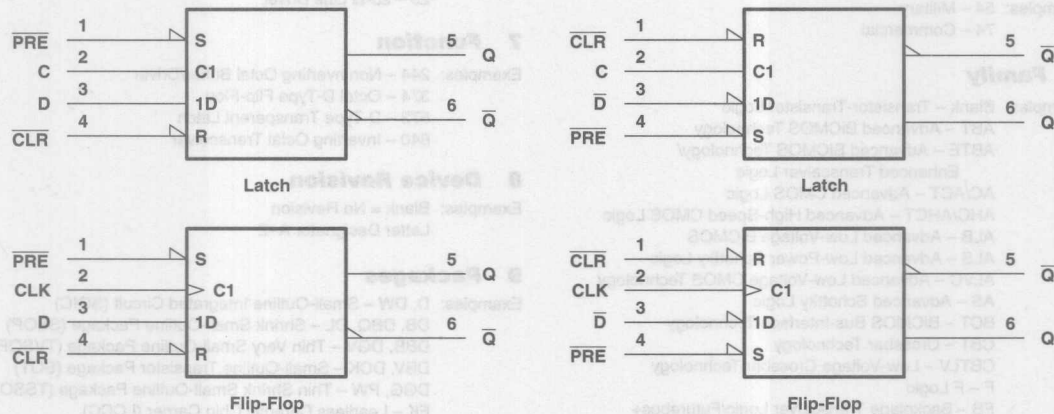


D FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \bar{Q} . An input that causes a Q output to go high or a \bar{Q} output to go low is called preset (PRE). An input that causes a \bar{Q} output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names (PRE and CLR) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits \bar{D} and Q.

In some applications, it may be advantageous to redesignate the data input from D to \bar{D} or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when Q and \bar{Q} exchange names, the preset and clear pins also exchange names. The polarity indicators (\triangle) on PRE and CLR remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or \bar{D}), Q, and \bar{Q} . Pin 5 (Q or \bar{Q}) is still in phase with the data input (D or \bar{D}); their active levels change together.

DEVICE NAMES AND PACKAGE DESIGNATORS

Example:

SN	74	LVT	H	16	2	244		DGG	R
1	2	3	4	5	6	7	8	9	10

1 Standard Prefix

Example: SNJ – Conforms to MIL-PRF-38535 (QML)

2 Temperature Range

Examples: 54 – Military
74 – Commercial

3 Family

Examples: Blank – Transistor-Transistor Logic
ABT – Advanced BiCMOS Technology
ABTE – Advanced BiCMOS Technology/
Enhanced Transceiver Logic
AC/ACT – Advanced CMOS Logic
AHC/AHCT – Advanced High-Speed CMOS Logic
ALB – Advanced Low-Voltage BiCMOS
ALS – Advanced Low-Power Schottky Logic
ALVC – Advanced Low-Voltage CMOS Technology
AS – Advanced Schottky Logic
BCT – BiCMOS Bus-Interface Technology
CBT – Crossbar Technology
CBTLV – Low-Voltage Crossbar Technology
F – F Logic
FB – Backplane Transceiver Logic/Futurebus+
GTL – Gunning Transceiver Logic
HC/HCT – High-Speed CMOS Logic
HSTL – High-Speed Transistor Logic
LS – Low-Power Schottky Logic
LV – Low-Voltage HCMOS Technology
LVC – Low-Voltage CMOS Technology
LVT – Low-Voltage BiCMOS Technology
S – Schottky Transistor-Transistor Logic
SSTL – Stub Series-Terminated Logic

4 Special Features

Examples: Blank – No Special Features
D – Level-Shifting Diode (CBTD)
H – Bus Hold (ALVCH)
R – Damping Resistor on Inputs/Outputs (LVCR)
S – Schottky Clamping Diode (CBTS)

5 Bit Width

Examples: Blank – Gates, MSI, and Octals
1G – Single Gate
8 – Octal IEEE 1149.1 (JTAG)
16 – Widebus™ (16, 18, and 20 bit)
18 – Widebus IEEE 1149.1 (JTAG)
32 – Widebus+™ (32 and 36 bit)

6 Options

Examples: Blank – No Options
2 – Series-Damping Resistor on Outputs
4 – Level Shifter
25 – 25-Ω Line Driver

7 Function

Examples: 244 – Noninverting Octal Buffer/Driver
374 – Octal D-Type Flip-Flop
573 – D-Type Transparent Latch
640 – Inverting Octal Transceiver

8 Device Revision

Examples: Blank – No Revision
Letter Designator A–Z

9 Packages

Examples: D, DW – Small-Outline Integrated Circuit (SOIC)
DB, DBQ, DL – Shrink Small-Outline Package (SSOP)
DBB, DGV – Thin Very Small-Outline Package (TVSOP)
DBV, DCK – Small-Outline Transistor Package (SOT)
DGG, PW – Thin Shrink Small-Outline Package (TSSOP)
FK – Leadless Ceramic Chip Carrier (LCCC)
FN – Plastic Leaded Chip Carrier (PLCC)
GB – Ceramic Pin Grid Array (CPGA)
HFP, HS, HT, HV – Ceramic Quad Flat Package (CQFP)
J, JT – Ceramic Dual-In-Line Package (CDIP)
N, NP, NT – Plastic Dual-In-Line Package (PDIP)
PAG, PAH, PCA, PCB, PM, PN, PZ –
Plastic Thin Quad Flat Package (TQFP)
PH, PQ, RC – Plastic Quad Flat Package (QFP)
W, WA, WD – Ceramic Flat Package (CFP)

10 Tape and Reel

Examples: Blank – Not Taped and Reeled
R – Reeled Product†

† All reeled material previously designated LE continues to be reeled left embossed, but an R designator is used.



General Information

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LVT Octals

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LVT Widebus™

3

Application Reports

4

Mechanical Data

5

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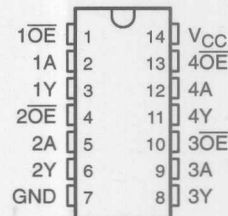
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SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

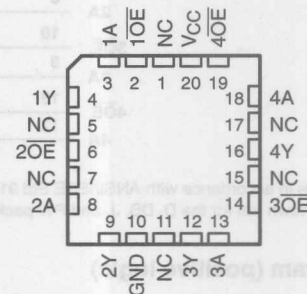
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH125 ... J PACKAGE
SN74LVTH125 ... D, DB, OR PW PACKAGE
(TOP VIEW)



SN54LVTH125 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus buffers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH125 devices feature independent line drivers with 3-state outputs. Each output is in the high-impedance state when the associated output-enable (\overline{OE}) input is high.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH125 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH125 is characterized for operation from -40°C to 85°C .

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SN54LVTH125, SN74LVTH125

3.3-V ABT QUADRUPLE BUS BUFFERS

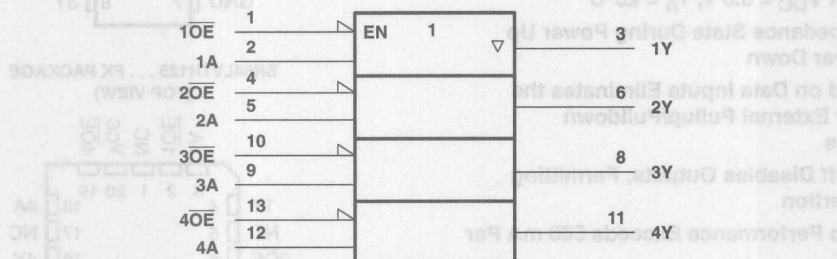
WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

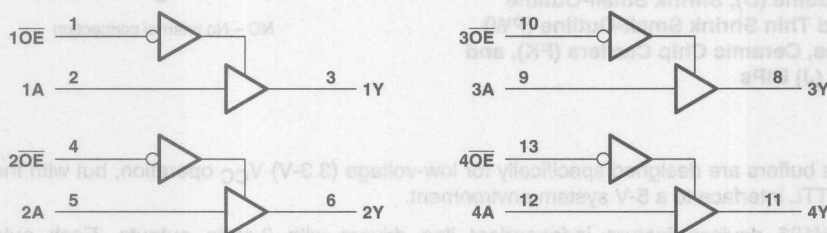
INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, and PW packages.

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SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH125	96 mA
SN74LVTH125	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH125	48 mA
SN74LVTH125	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package	127°C/W
DB package	158°C/W
PW package	170°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH125		SN74LVTH125		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

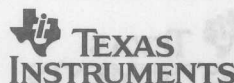
PARAMETER		TEST CONDITIONS		SN54LVTH125			SN74LVTH125			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2			-1.2	V
V _{OH}		V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2			V
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4			2.4			
		V _{CC} = 3 V	I _{OH} = -24 mA	2						
			I _{OH} = -32 mA				2			
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2			0.2	V
			I _{OL} = 24 mA			0.5		0.5		
		V _{CC} = 3 V	I _{OL} = 16 mA			0.4		0.4		
			I _{OL} = 32 mA			0.5		0.5		
			I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA			0.55				
I _I	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10			10	μA	
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1		±1		
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}			1		1		
			V _I = 0			-5		-5		
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V					±100	μA	
I _I (hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75			μA	
			V _I = 2 V	-75		-75				
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5		5	μA	
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			-5		-5	μA	
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care					±50*		±50	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care					±50*		±50	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		4.5	7		4.5	7	
			Outputs disabled		0.12	0.19		0.12	0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.3		0.2	mA
C _I		V _I = 3 V or 0					4		4	pF
C _O		V _O = 3 V or 0					8		8	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC} \text{ or GND}$.

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SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH125				SN74LVTH125				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t _{PLH}	A	Y	1	4.2		4.7	1	2	3.5		4.5	ns
t _{PHL}			1	4.1		5.1	1	2.1	3.9		4.9	
t _{PZH}	OE	Y	1	4.9		5.6	1	2	4		5.5	ns
t _{PZL}			1.1	4.9		5.6	1.1	2.1	4		5.4	
t _{PHZ}	OE	Y	1.5	5.3		5.9	1.5	2.3	4.5		5.7	ns
t _{PLZ}			1.3	4.7		4.2	1.3	2.8	4.5		4	

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

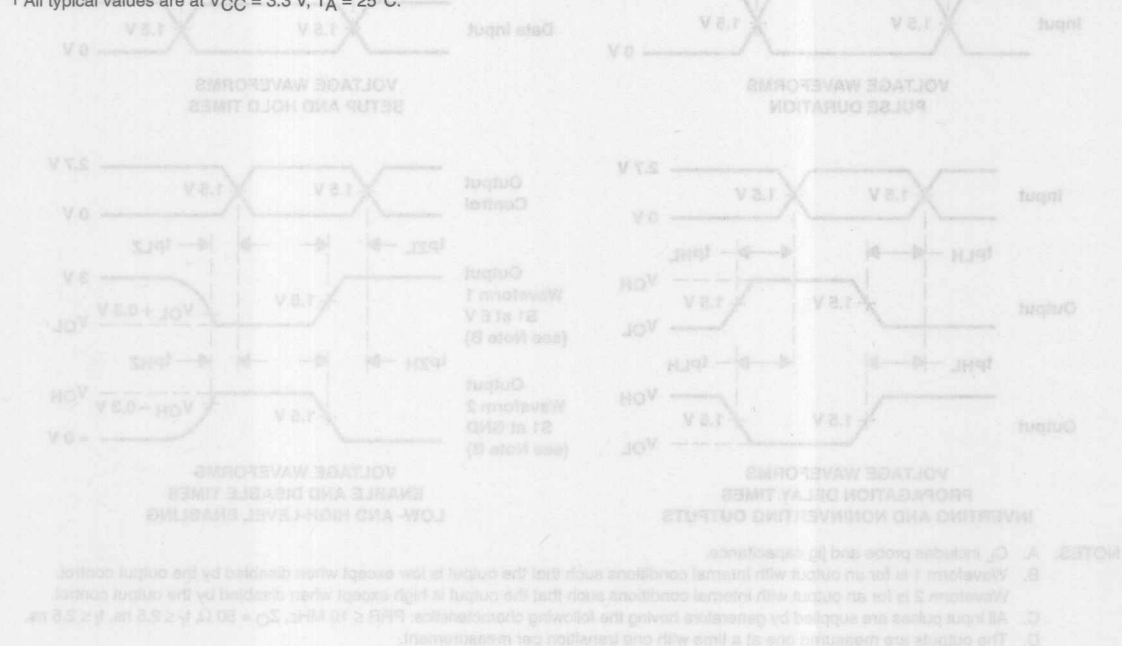


Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

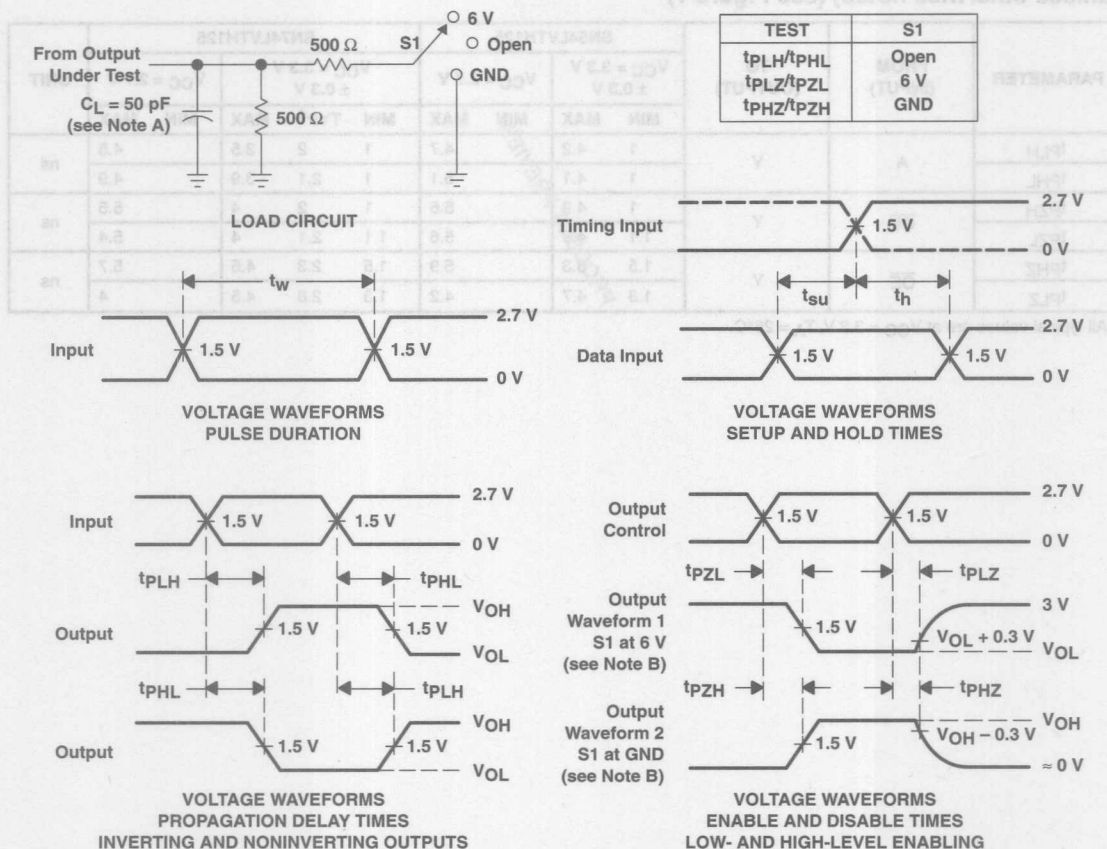
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SN54LVTH125, SN74LVTH125 3.3-V ABT QUADRUPLE BUS BUFFERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

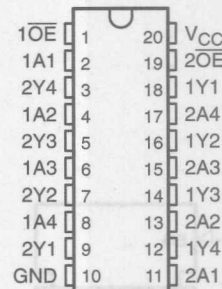
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

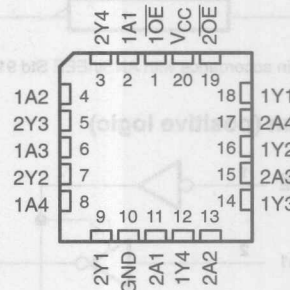
SCBS679C – DECEMBER 1996 – REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH240 ... J PACKAGE
SN74LVTH240 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH240 ... FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are organized as two 4-bit buffer/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the devices pass data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH240 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH240 is characterized for operation from -40°C to 85°C .

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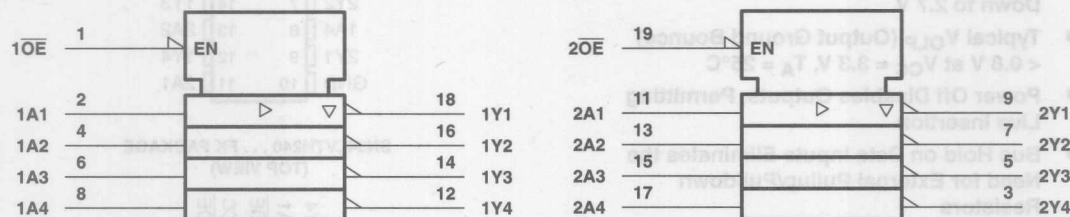
SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

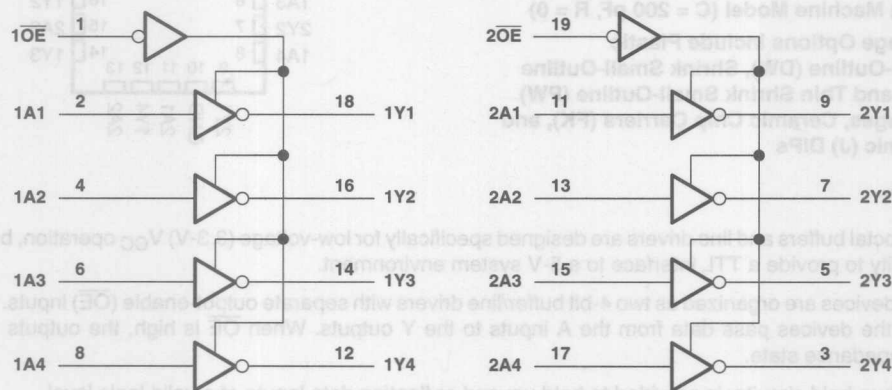
INPUTS		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH240, SN74LVTH240

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS679C – DECEMBER 1996 – REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH240	96 mA
SN74LVTH240	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH240	48 mA
SN74LVTH240	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH240		SN74LVTH240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH240, SN74LVTH240 **3.3-V ABT OCTAL BUFFERS/DRIVERS** **WITH 3-STATE OUTPUTS**

SCBS679C – DECEMBER 1996 – REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH240			SN74LVTH240			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$		2					
					2			
V_{OL}	$V_{CC} = 2.7\text{ V}$			0.2			0.2	V
				0.5			0.5	
				0.4			0.4	
	$V_{CC} = 3\text{ V}$			0.5			0.5	
				0.55				
							0.55	
I_I		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	μA
	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6\text{ V}$, $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			3			3	pF
C_o	$V_O = 3\text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS679C – DECEMBER 1996 – REVISED MARCH 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH240				SN74LVTH240				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t _{PLH}	A	Y	1	3.9		4.7	1.1	2.2	3.8		4.6	ns
t _{PHL}			1.2	4.2		4.3	1.3	2.6	4		4.2	
t _{PZH}	OE	Y	1	4.7		5.7	1.1	2.6	4.6		5.6	ns
t _{PZL}			1.3	4.6		5.2	1.4	2.7	4.4		5	
t _{PHZ}	OE	Y	1.9	4.6		4.8	2	2.9	4.4		4.6	ns
t _{PLZ}			1.7	4.7		4.7	1.8	3	4.3		4.3	

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

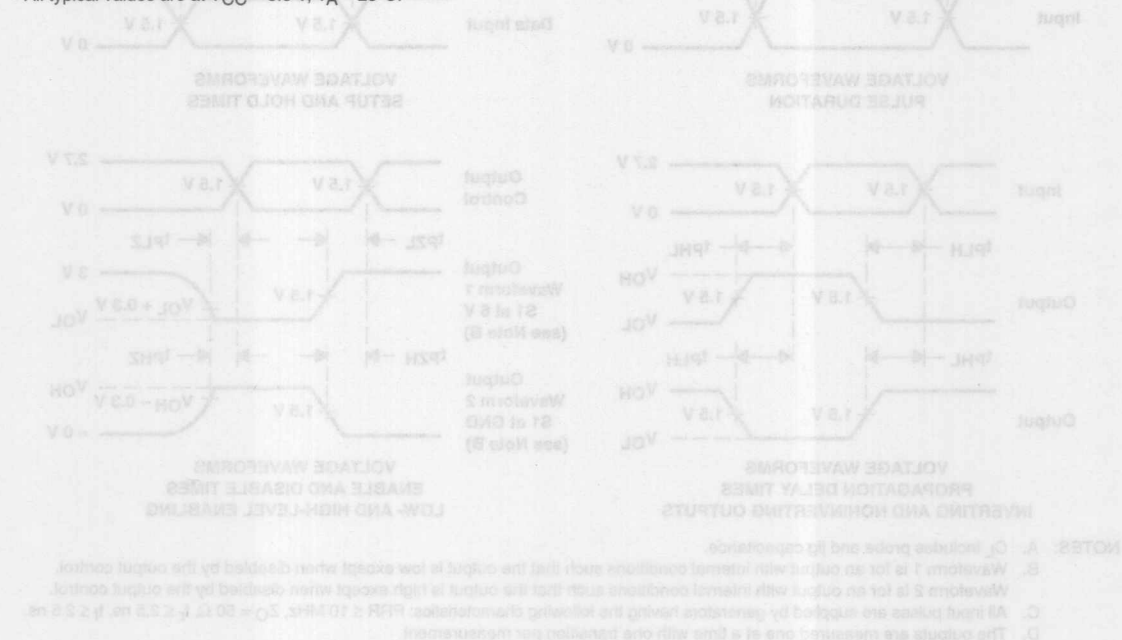


Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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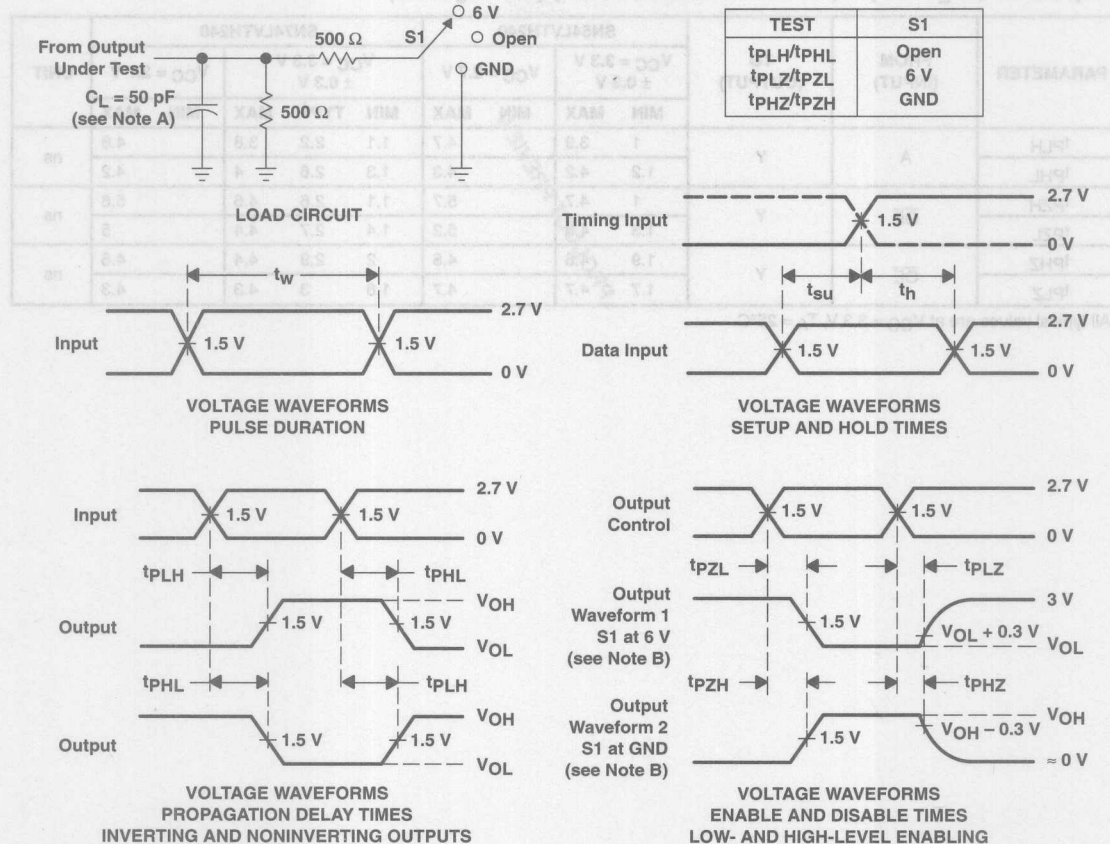
SN54LVTH240, SN74LVTH240

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS679C – DECEMBER 1996 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

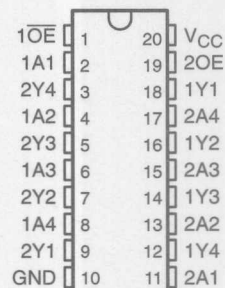
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

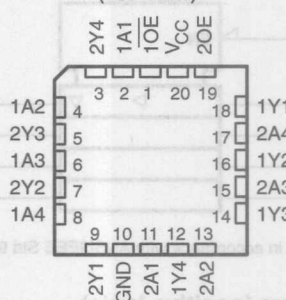
SCAS352H – MARCH 1994 – REVISED APRIL 1998

- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH241 ... J PACKAGE
SN74LVTH241 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH241 ... FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH241 devices are organized as two 4-bit line drivers with separate output-enable ($1\overline{OE}$, $2OE$) inputs. When $1\overline{OE}$ is low or $2OE$ is high, the devices pass noninverted data from the A inputs to the Y outputs. When $1\overline{OE}$ is high or $2OE$ is low, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH241 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH241 is characterized for operation from -40°C to 85°C .

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

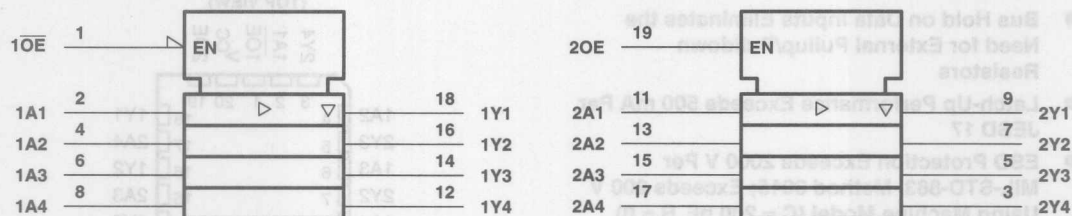
SCAS352H – MARCH 1994 – REVISED APRIL 1998

FUNCTION TABLES

INPUTS		OUTPUT
1OE	1A	1Y
L	H	H
L	L	L
H	X	Z

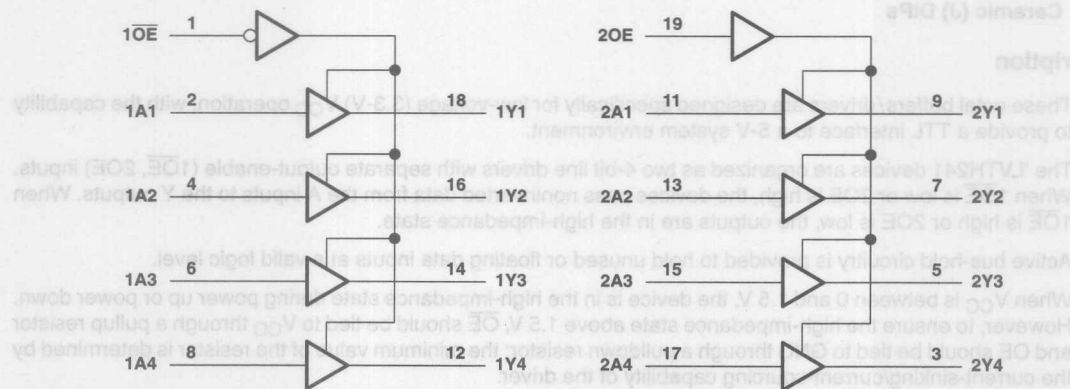
INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS352H – MARCH 1994 – REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH241	96 mA
SN74LVTH241	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH241	48 mA
SN74LVTH241	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

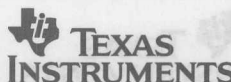
- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH241		SN74LVTH241		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS352H – MARCH 1994 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH241		SN74LVTH241		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2		-1.2	V	
V _{OH}		V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2			V	
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4				
		V _{CC} = 3 V	I _{OH} = -24 mA	2						
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2		0.2	V	
			I _{OL} = 24 mA			0.5		0.5		
		V _{CC} = 3 V	I _{OL} = 16 mA			0.4		0.4		
			I _{OL} = 32 mA			0.5		0.5		
			I _{OL} = 48 mA			0.55				
			I _{OL} = 64 mA					0.55		
I _I	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10		10	μA		
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1			±1	
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC} V _I = 0			1 -5			1 -5	
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V					±100	μA	
I _I (hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75			μA	
			V _I = 2 V	-75		-75				
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5		5	μA	
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			-5		-5	μA	
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE/OE = don't care					±100*		±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE/OE = don't care					±100*		±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			0.19		0.19	mA	
			Outputs low			5		5		
			Outputs disabled			0.19		0.19		
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2		0.2	mA
C _I		V _I = 3 V or 0					3		3	pF
C _O		V _O = 3 V or 0					7		7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS352H - MARCH 1994 - REVISED APRIL 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH241				SN74LVTH241				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1	3.7	4		1.1	2.3	3.5	3.9		ns
t _{PHL}			1.2	3.5	3.7		1.3	2.2	3.4	3.6		
t _{PZH}	\overline{OE} or OE	Y	1	4.6	5.5		1.1	2.7	4.5	5.4		ns
t _{PZL}			1.3	4.6	5.1		1.4	2.9	4.4	5		
t _{PHZ}	\overline{OE} or OE	Y	1.5	4.7	5.5		1.6	2.8	4.5	5.3		ns
t _{PLZ}			1.7	5	5.5		1.8	3	4.7	5.2		

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

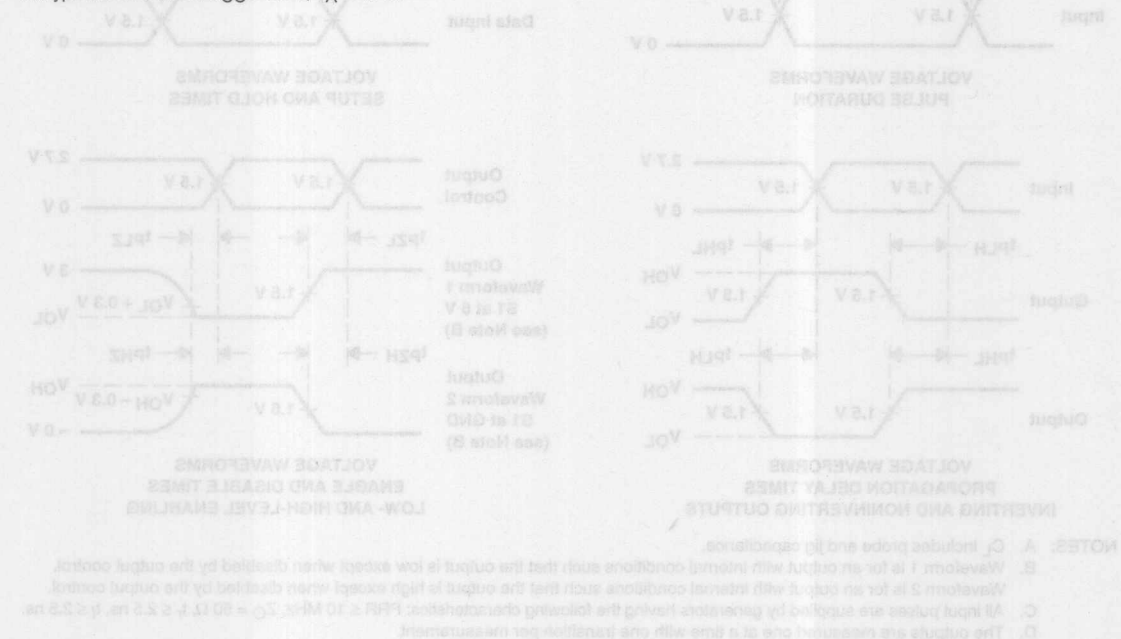


Figure 1. Load Circuit and Voltage Waveforms

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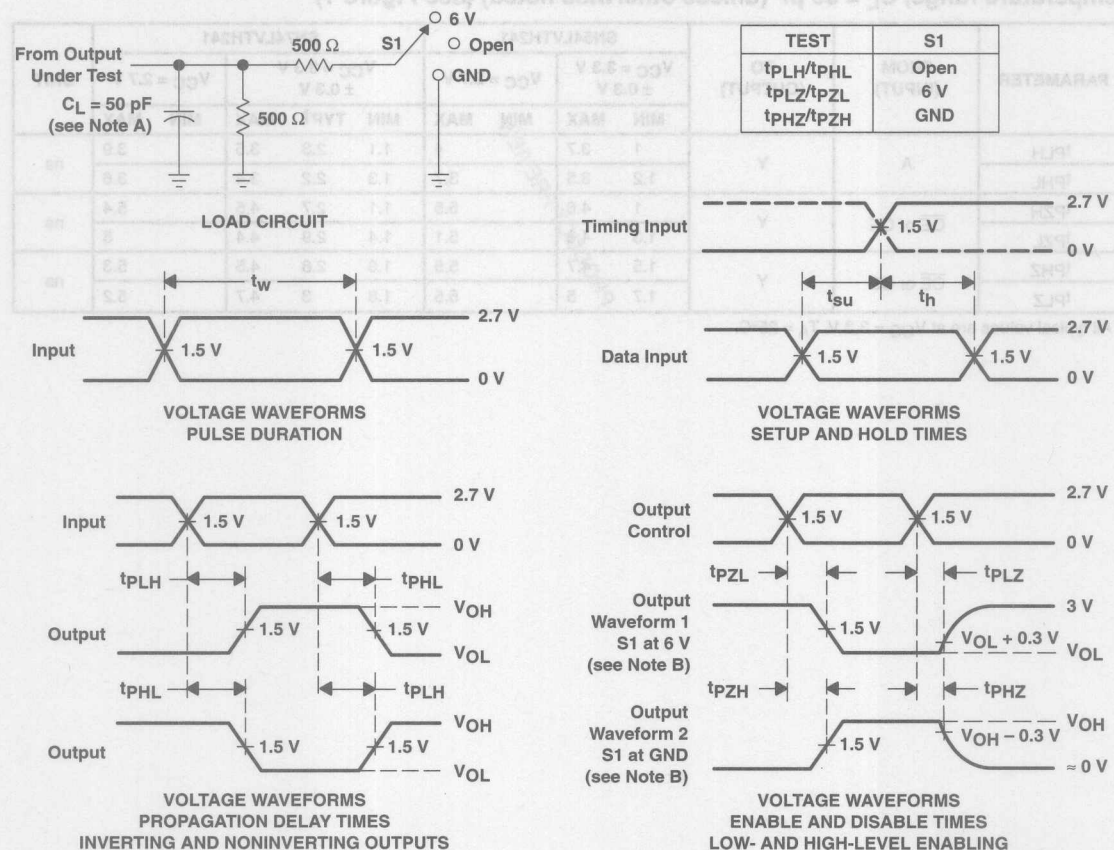


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SN54LVTH241, SN74LVTH241 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS352H – MARCH 1994 – REVISED APRIL 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

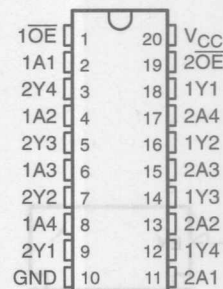
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

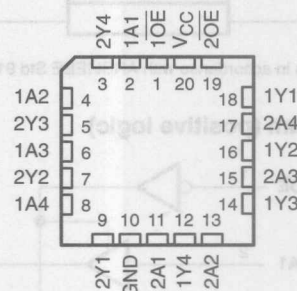
SCAS586C – DECEMBER 1996 – REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVTH244A ... J OR W PACKAGE
SN74LVTH244A ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH244A ... FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH244A devices are organized as two 4-bit line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH244A is characterized for operation from -40°C to 85°C .

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SN54LVTH244A, SN74LVTH244A

3.3-V ABT OCTAL BUFFERS/DRIVERS

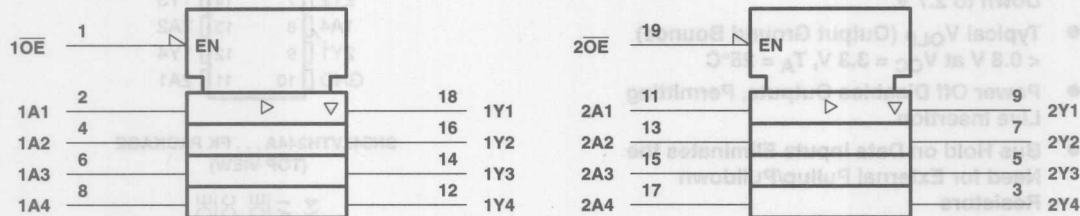
WITH 3-STATE OUTPUTS

SCAS586C - DECEMBER 1996 - REVISED MARCH 1998

FUNCTION TABLE
(each buffer)

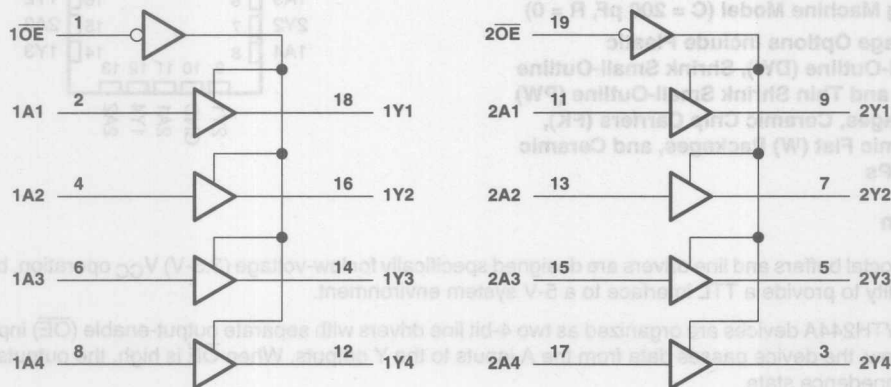
INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS586C – DECEMBER 1996 – REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH244A	96 mA
SN74LVTH244A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH244A	48 mA
SN74LVTH244A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH244A		SN74LVTH244A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH244A, SN74LVTH244A **3.3-V ABT OCTAL BUFFERS/DRIVERS** **WITH 3-STATE OUTPUTS**

SCAS586C – DECEMBER 1996 – REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH244A			SN74LVTH244A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$I_{OH} = -24\text{ mA}$	2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4			0.4	
		$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$		0.55				
		$I_{OL} = 64\text{ mA}$					0.55	
I_I	$V_{CC} = 0\text{ or } 3.6\text{ V}$, Control inputs	$V_I = 5.5\text{ V}$		10			10	μA
	$V_{CC} = 3.6\text{ V}$, Data inputs	$V_I = V_{CC}\text{ or GND}$		± 1			± 1	
	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$ $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_{I(hold)}$	A inputs	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_I = 2\text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			3			3	pF
C_o	$V_O = 3\text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.



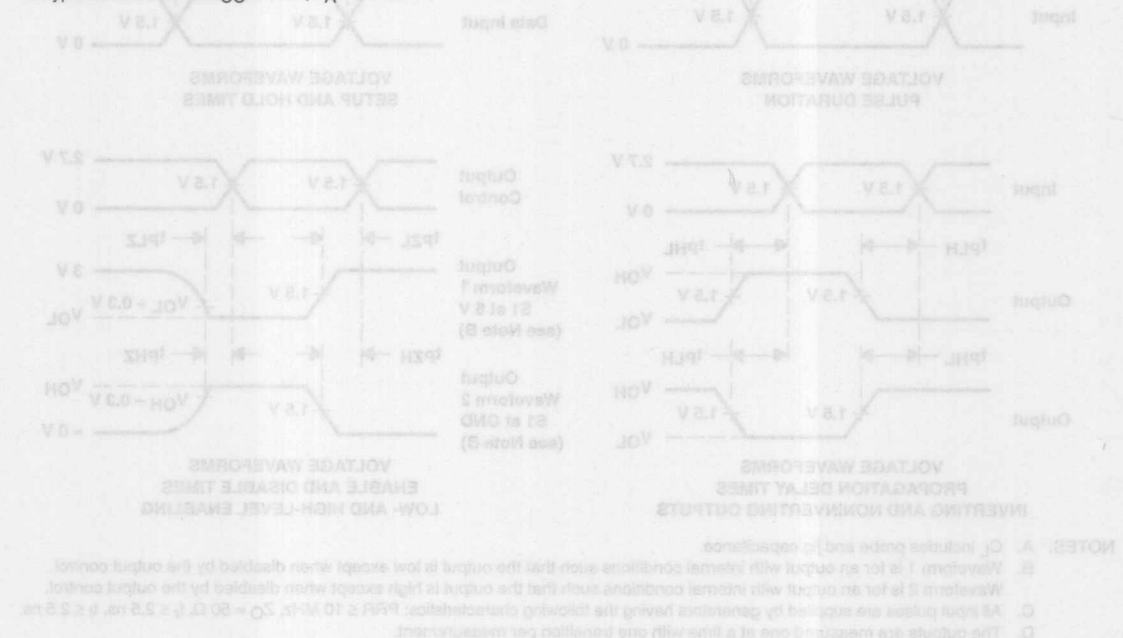
SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCAS586C – DECEMBER 1996 – REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH244A				SN74LVTH244A				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t _{PLH}	A	Y	1	3.6		4.1	1.1	2.3	3.5		3.8	ns
t _{PHL}			1.2	3.4		3.9	1.3	2.1	3.3		3.6	
t _{PZH}	\overline{OE}	Y	1	6.9		6	1.1	2.5	4.5		5.3	ns
t _{PZL}			1.3	4.5		5.4	1.4	2.7	4.4		4.9	
t _{PHZ}	\overline{OE}	Y	1.3	4.5		5.8	1.9	2.8	4.4		4.5	ns
t _{PLZ}			1.2	4.5		4.8	1.8	2.9	4.4		4.4	

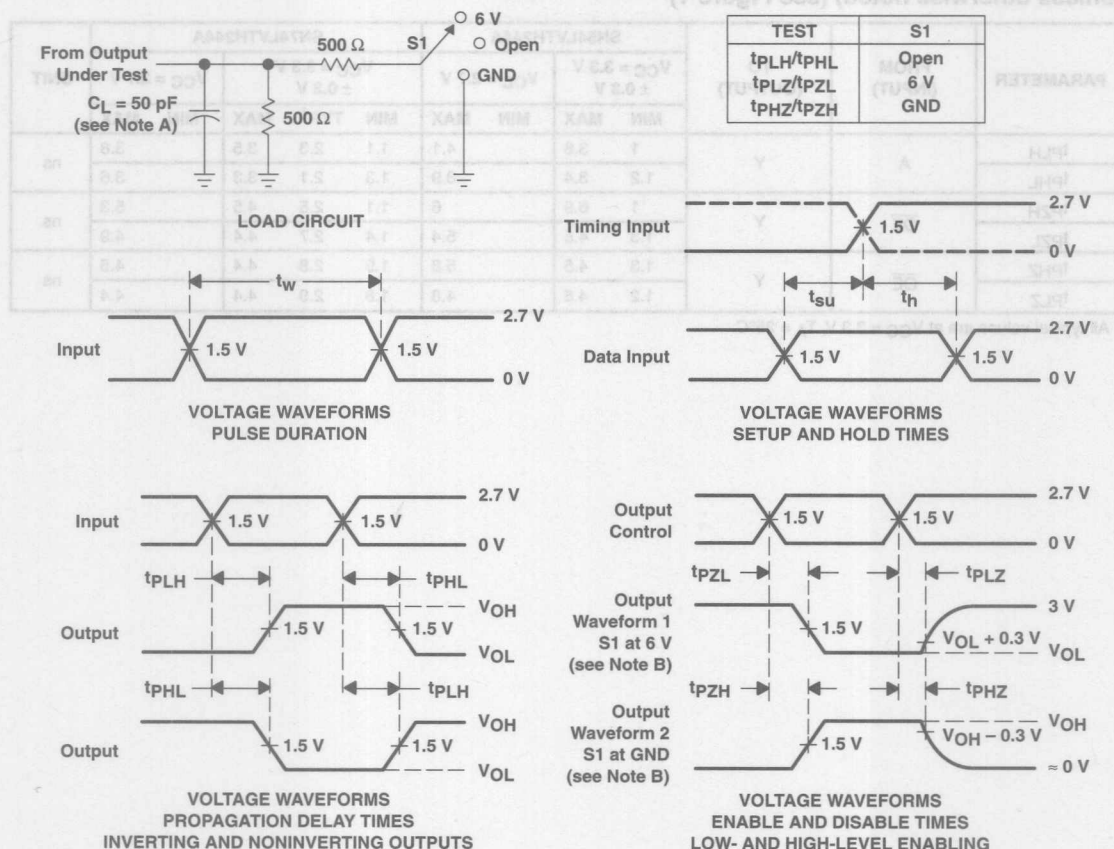
† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.



SN54LVTH244A, SN74LVTH244A 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

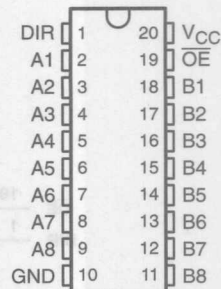
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH245A, SN74LVTH245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

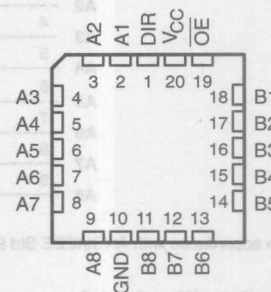
SCBS1300 – MAY 1992 – REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVTH245A ... J OR W PACKAGE
SN74LVTH245A ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH245A ... FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.


These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH245A is characterized for operation from -40°C to 85°C .

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH245A, SN74LVTH245A

3.3-V ABT OCTAL BUS TRANSCEIVERS

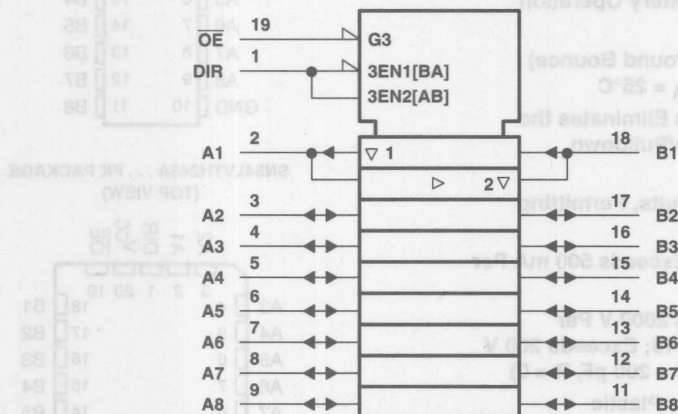
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

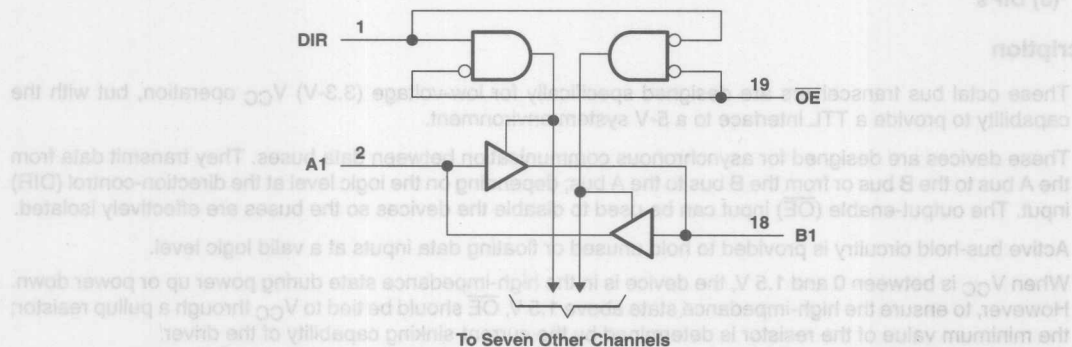
INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

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**TEXAS
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SN54LVTH245A, SN74LVTH245A

3.3-V ABT OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS1300 - MAY 1992 - REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH245A	96 mA
SN74LVTH245A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH245A	48 mA
SN74LVTH245A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH245A		SN74LVTH245A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH245A, SN74LVTH245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

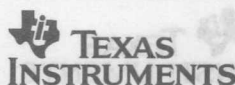
PARAMETER	TEST CONDITIONS	SN54LVTH245A			SN74LVTH245A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4			0.4	
		$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$		0.55				
		$I_{OL} = 64\text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		20			20	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $OE = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $OE = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			4			4	pF
C_{io}	$V_O = 3\text{ V or } 0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals are at $V_{CC}\text{ or GND}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.



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SN54LVTH245A, SN74LVTH245A 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS1300 – MAY 1992 – REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH245A				SN74LVTH245A				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A or B	B or A	0.7	3.7		4.2	1.2	2.3	3.5		4	ns
t _{PHL}			0.7	3.7		4.2	1.2	2.1	3.5		4	
t _{PZH}	\overline{OE}	A or B	1.2	5.7		7.4	1.3	3.2	5.5		7.1	ns
t _{PZL}			1.6	5.7		6.8	1.7	3.4	5.5		6.5	
t _{PHZ}	\overline{OE}	A or B	1.8	6.2		6.8	2.2	3.5	5.9		6.5	ns
t _{PLZ}			1.8	5.3		5.5	2.2	3.4	5		5.1	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

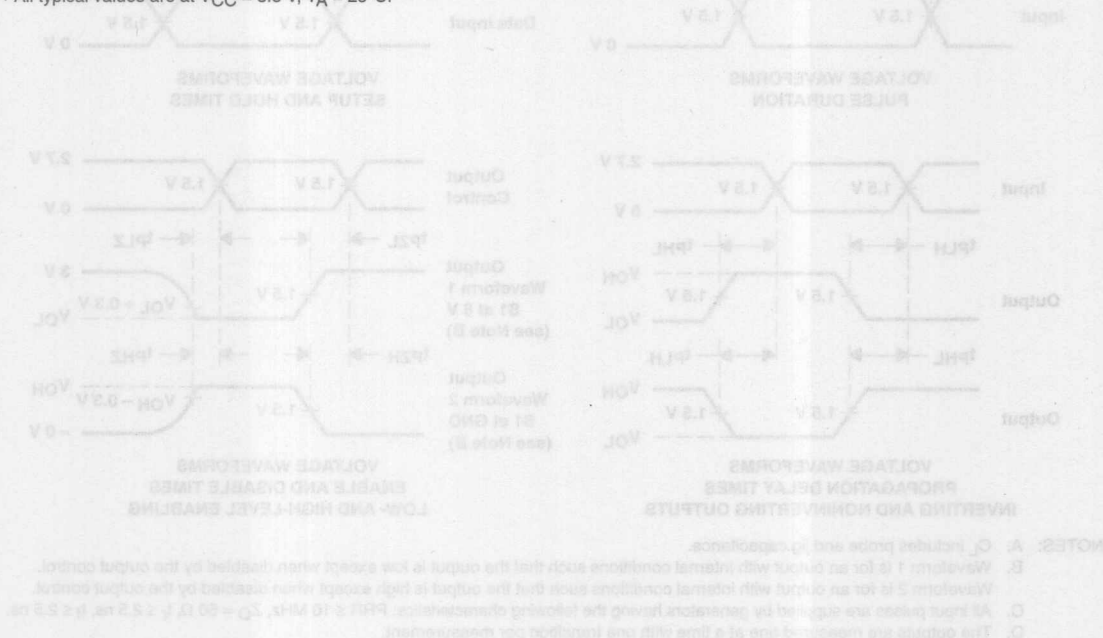


Figure 1. Load Circuit and Voltage Waveforms

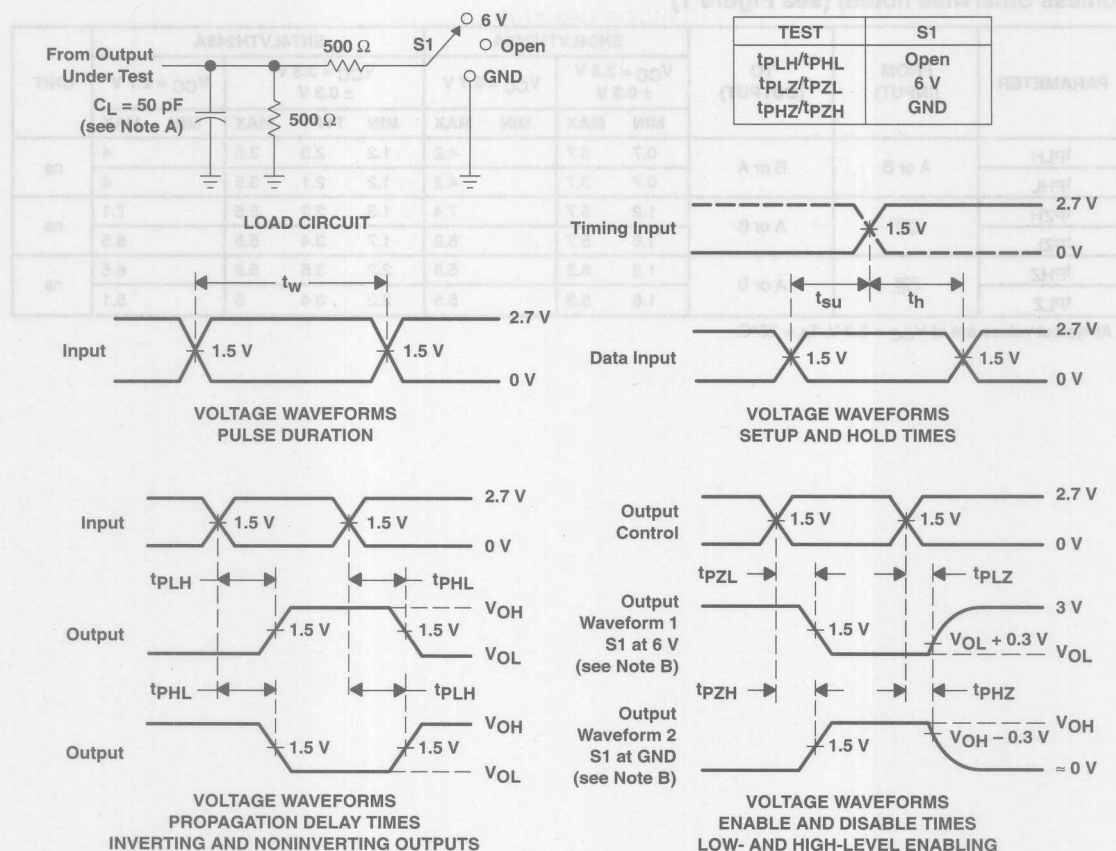
SN54LVTH245A, SN74LVTH245A

3.3-V ABT OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS1300 – MAY 1992 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

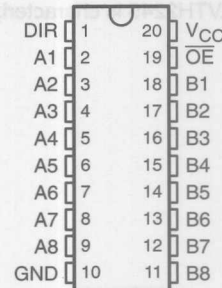


SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

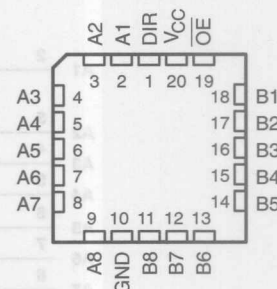
SCBS707B – SEPTEMBER 1997 – REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- B-Port Outputs Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required
- High-Impedance State During Power Up and Power Down
- Power Off Disables Outputs, Permitting Live Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Packages, and Ceramic (J) DIPs

SN54LVTH2245 ... J OR W PACKAGE
SN74LVTH2245 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH2245 ... FK PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are designed for asynchronous communication between data buses. They transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The B-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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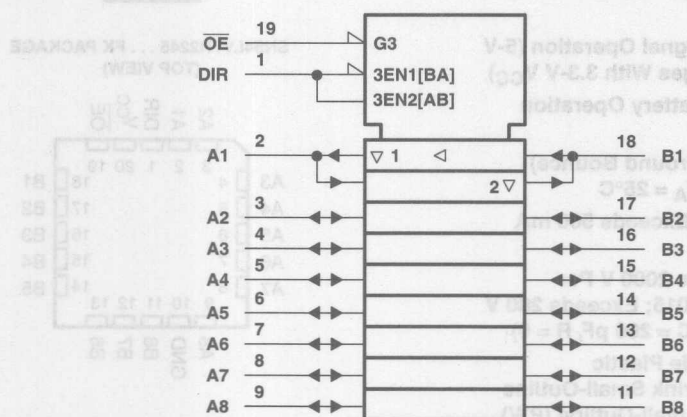
description (continued)

The SN54LVTH2245 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74LVTH2245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

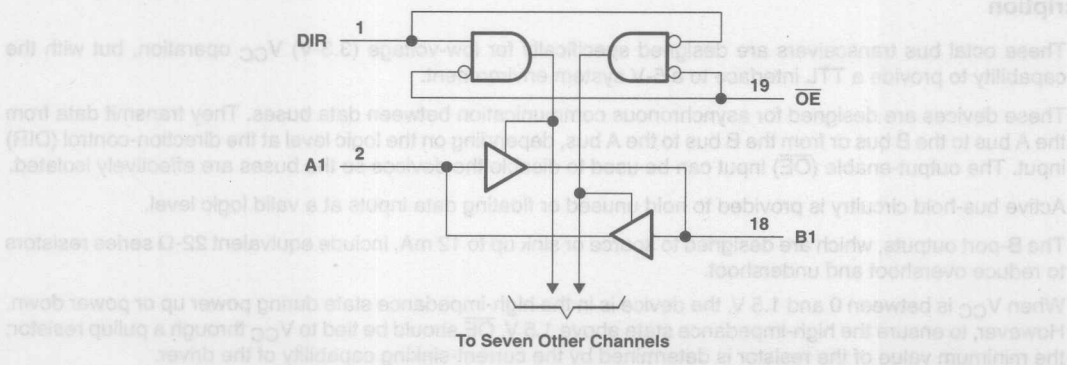
INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH2245 (A port)	96 mA
SN74LVTH2245 (A port)	128 mA
B port	30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH2245 (A port)	48 mA
SN74LVTH2245 (A port)	64 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH2245		SN74LVTH2245		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current	A port	–24		–32	mA
		B port	–12		–12	
I _{OL}	Low-level output current	A port	48		64	mA
		B port	12		12	
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH2245, SN74LVTH2245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH2245			SN74LVTH2245			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	A port	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$	$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4	2.4			
		$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2				
	B port	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$	$V_{CC}-0.2$			V
		$V_{CC} = 3\text{ V}$, $I_{OH} = -12\text{ mA}$		2	2			
V_{OL}	A port	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2	V
			$I_{OL} = 24\text{ mA}$		0.5		0.5	
			$I_{OL} = 16\text{ mA}$		0.4		0.4	
		$V_{CC} = 3\text{ V}$	$I_{OL} = 32\text{ mA}$		0.5		0.5	
			$I_{OL} = 48\text{ mA}$		0.55		0.55	
			$I_{OL} = 64\text{ mA}$				0.55	
	B port	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2		V
		$V_{CC} = 3\text{ V}$, $I_{OL} = 12\text{ mA}$		0.8		0.8		
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1		± 1		μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10		10		
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		20		20		
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		1		1		
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		-5		-5		
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		-5		-5		
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$				± 100		μA
$I_{I(\text{hold})}$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75		75		μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$		-75		-75		
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $O\bar{E} = \text{don't care}$		$\pm 100^*$		± 100		μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $O\bar{E} = \text{don't care}$		$\pm 100^*$		± 100		μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19		0.1	0.19	mA
			Outputs low	5		3	5	
			Outputs disabled	0.19		0.1	0.19	
$\Delta I_{CC}\S$		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2		0.2		mA
C_i		$V_I = 3\text{ V or } 0$		4		4		pF
C_{io}		$V_O = 3\text{ V or } 0$		9		9		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals are at $V_{CC}\text{ or GND}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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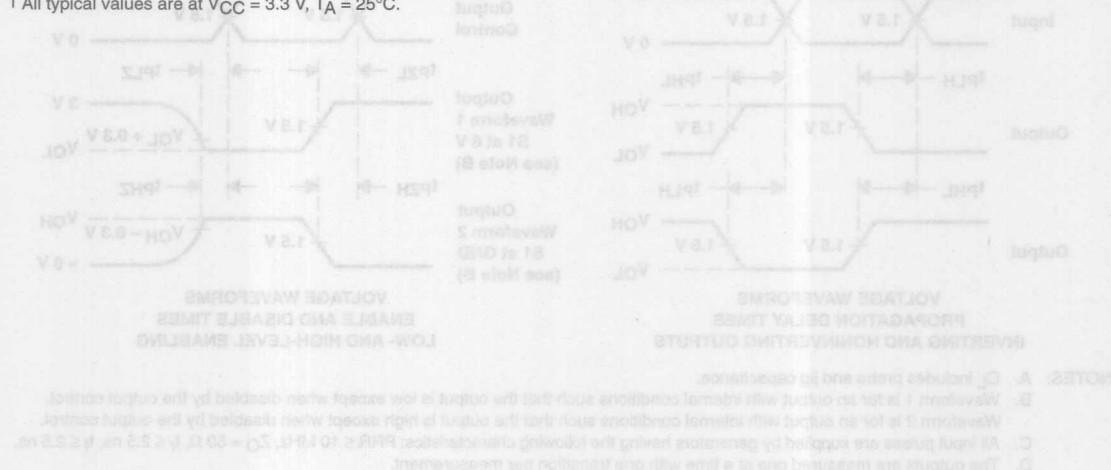
SN54LVTH2245, SN74LVTH2245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS707B – SEPTEMBER 1997 – REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH2245				SN74LVTH2245				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	B	1	4.6		5.3	1.1	2.9	4.4		5.1	ns
t _{PHL}			1	4.6		5.3	1.1	2.6	4.4		5.1	
t _{PLH}	B	A	1	3.7		4.2	1.1	2.2	3.5		4	ns
t _{PHL}			1	3.7		4.2	1.1	2	3.5		4	
t _{PZH}	OE	A	1.2	5.7		7.4	1.3	3.1	5.5		7.1	ns
t _{PZL}			1.6	5.7		6.8	1.7	3.2	5.5		6.5	
t _{PHZ}	OE	A	2	6.2		6.8	2.2	3.6	5.9		6.5	ns
t _{PLZ}			2	5.3		5.5	2.2	3.4	5		5.1	
t _{PZH}	OE	B	1.2	6.4		7.6	1.3	3.5	6.2		7.3	ns
t _{PZL}			1.6	6.4		7.5	1.7	3.7	6.2		7.3	
t _{PHZ}	OE	B	2	6.1		6.8	2.2	3.9	5.9		6.5	ns
t _{PLZ}			2	5.7		5.9	2.2	3.7	5.4		5.7	

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.



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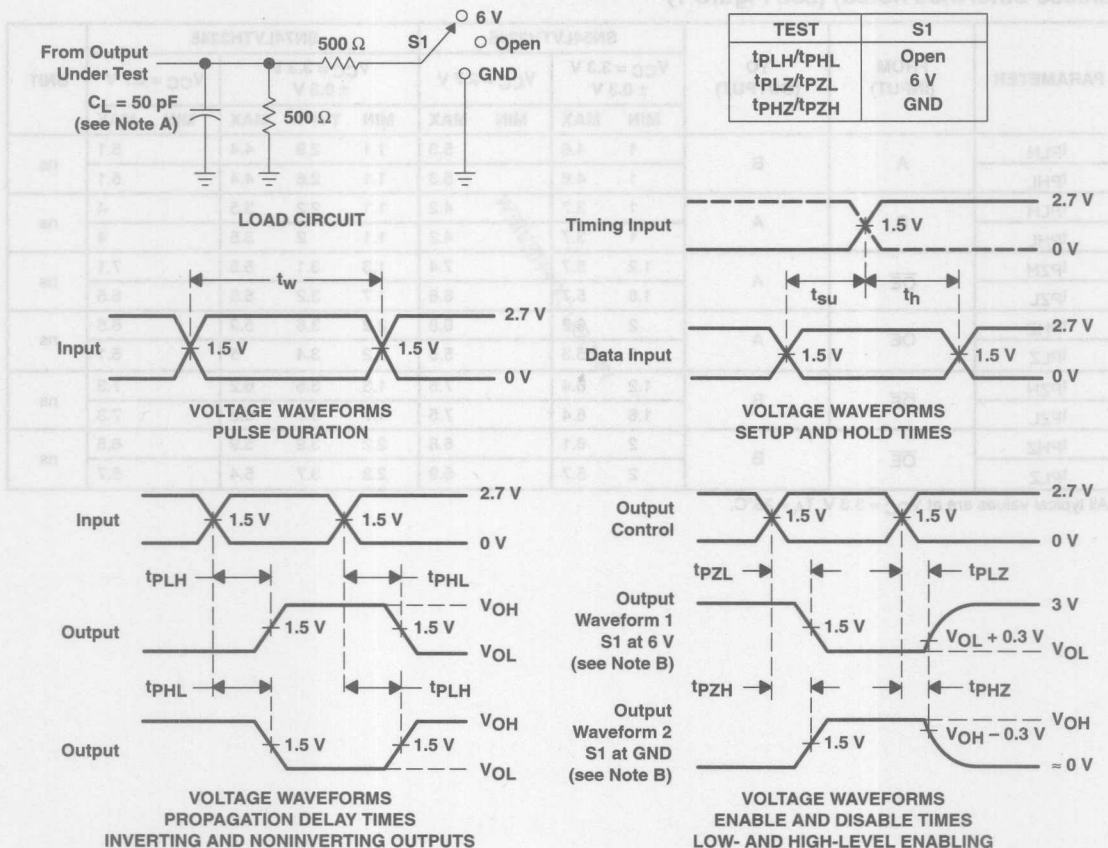


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SN54LVTH2245, SN74LVTH2245
3.3-V ABT OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

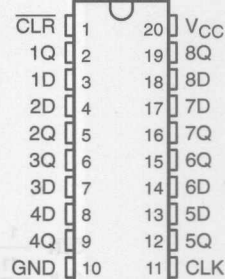
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

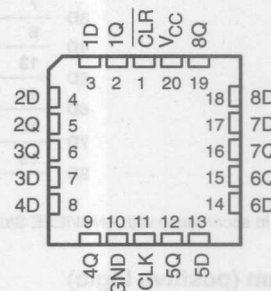
SCBS136J – MAY 1992 – REVISED APRIL 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (J) DIPs

SN54LVTH273 ... J PACKAGE
SN74LVTH273 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH273 ... FK PACKAGE
(TOP VIEW)



description

These octal D-type flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The LVTH273 devices are positive-edge-triggered flip-flops with a direct clear input. Information at the data (D) inputs meeting the setup-time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH273 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH273 is characterized for operation from -40°C to 85°C .

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**TEXAS
INSTRUMENTS**

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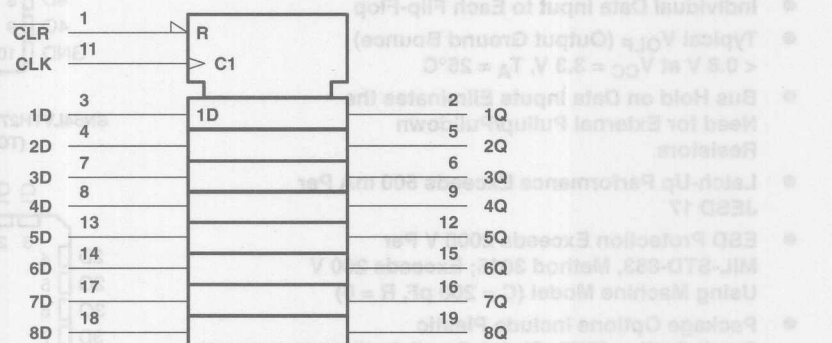
SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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FUNCTION TABLE
(each flip-flop)

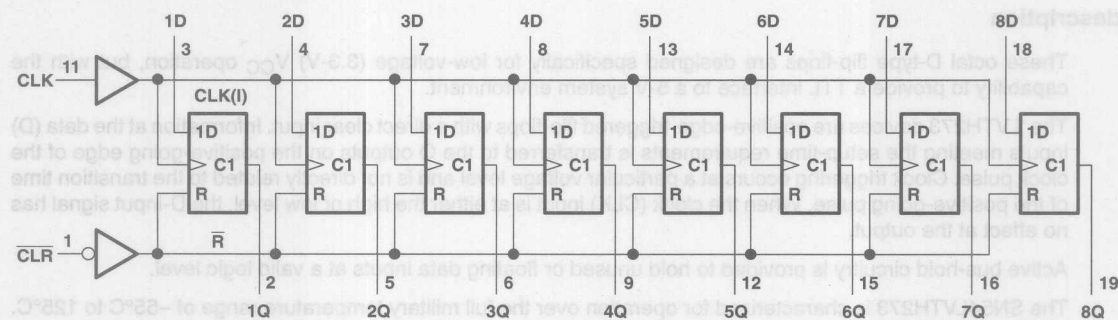
INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	H or L	X	Q ₀

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH273	96 mA
SN74LVTH273	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH273	48 mA
SN74LVTH273	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH273		SN74LVTH273		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH273			SN74LVTH273			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4			0.4	
		$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$		0.55			0.55	
		$I_{OL} = 64\text{ mA}$					0.55	
I_I	$V_{CC} = 0\text{ or } 3.6\text{ V}$, Control inputs	$V_I = 5.5\text{ V}$		10			10	μA
	$V_{CC} = 3.6\text{ V}$, Data inputs	$V_I = V_{CC}\text{ or GND}$		± 1			± 1	
	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$ $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75			75	μA
		$V_I = 2\text{ V}$		-75			-75	
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			4			4	pF

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH273				SN74LVTH273				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		150				150				MHz
t_w	Pulse duration		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	Data high or low before CLK↑	2.3		2.7		2.3		2.7		ns
		CLR high before CLK↑	2.3		2.7		2.3		2.7		
t_h	Hold time, data high or low after CLK↑		0		0		0		0		ns

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SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH273				SN74LVTH273				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150				150				MHz	
t _{PLH}	CLK	Any Q	1.6	5		5.6	1.7	3.2	4.9		5.5	ns
t _{PHL}			1.8	4.9		5.2	1.9	3.2	4.8		5.1	
t _{PHL}	CLR	Any Q	1.5	4.4		4.8	1.6	2.7	4.3		4.7	ns

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

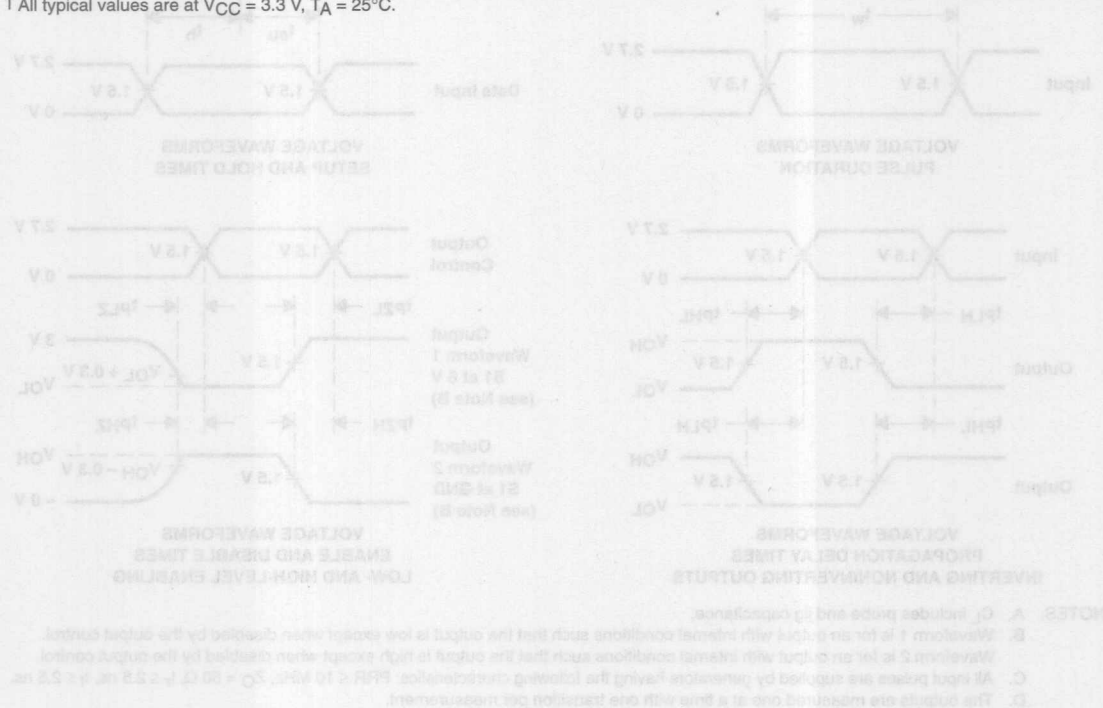


Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

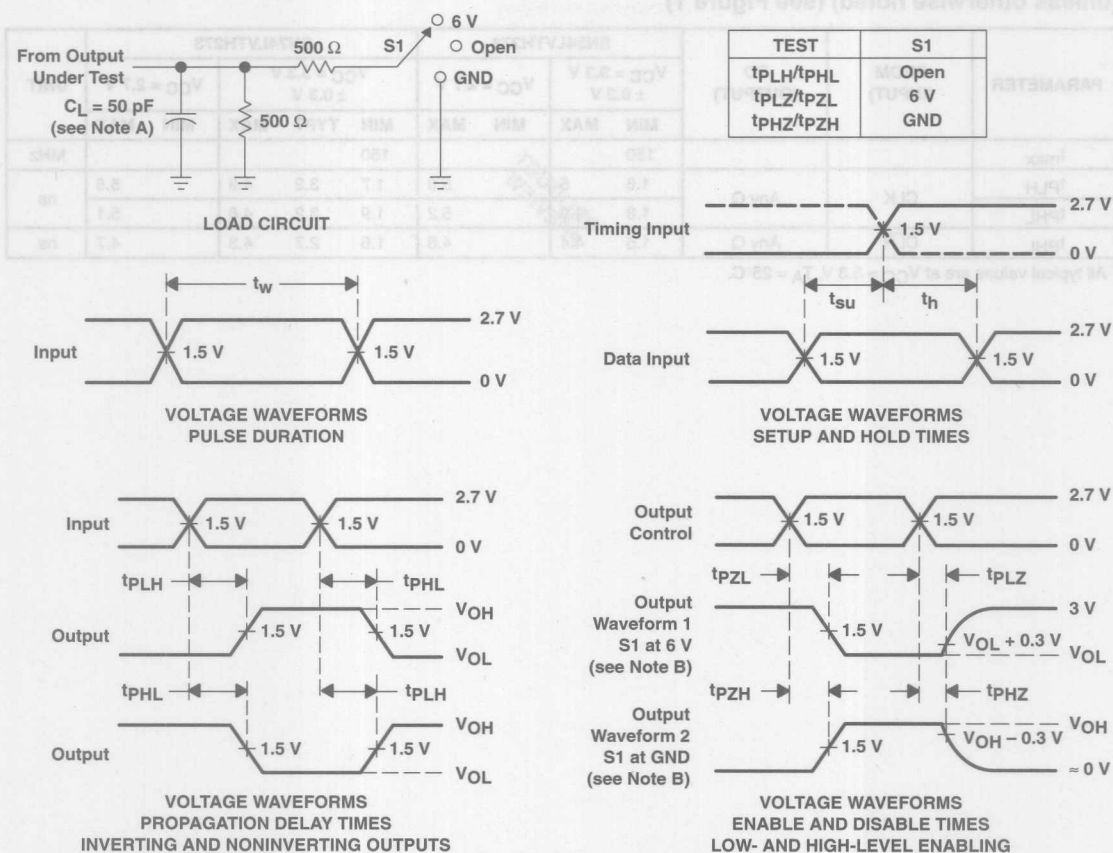


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SN54LVTH273, SN74LVTH273 3.3-V ABT OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

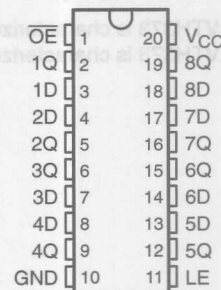
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

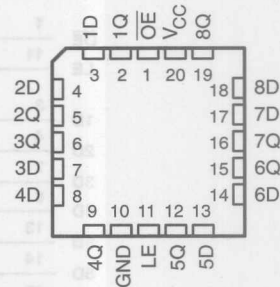
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH373 ... J OR W PACKAGE
SN74LVTH373 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH373 ... FK PACKAGE
(TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SN54LVTH373, SN74LVTH373 **3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES** **WITH 3-STATE OUTPUTS**

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

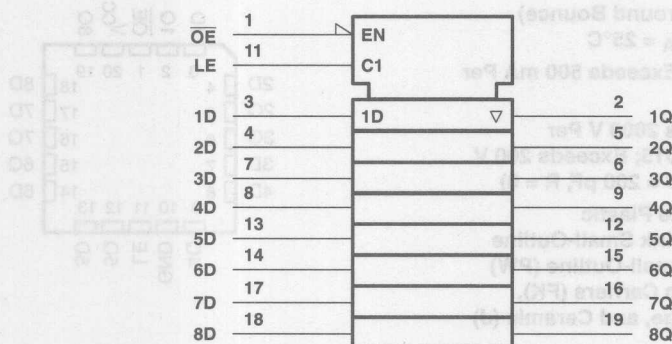
The SN54LVTH373 is characterized for operation over the full military temperature range of -55°C to 125°C .

The SN74LVTH373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

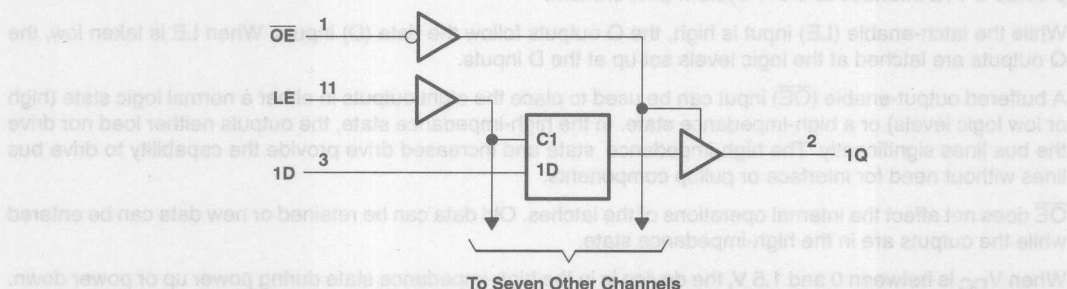
INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH373	96 mA
SN74LVTH373	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH373	48 mA
SN74LVTH373	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

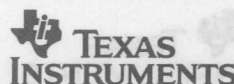
- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH373		SN74LVTH373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH373, SN74LVTH373
3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH373			SN74LVTH373			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$		0.5			0.5	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4			0.4	
		$I_{OL} = 32 \text{ mA}$		0.5			0.5	
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		10			10	μA
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75		75			μA
		$V_I = 2 \text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\text{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\text{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			± 0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$			3			3	pF
C_o	$V_O = 3 \text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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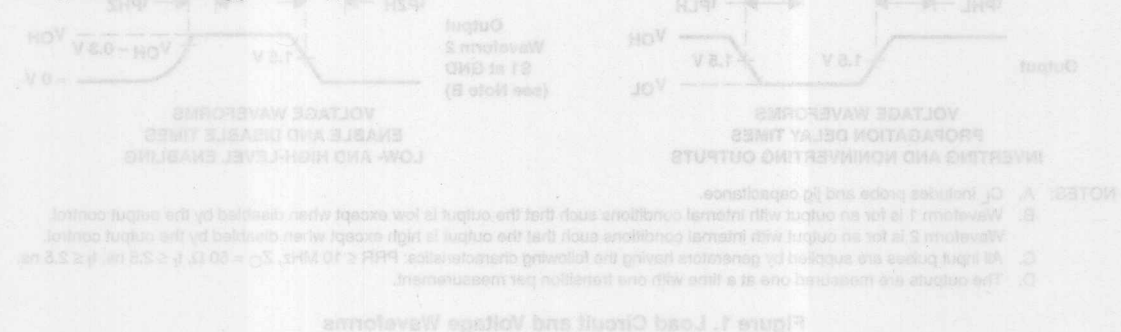
timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH373				SN74LVTH373				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	3		3		3		3		ns
t_{SU}	Setup time, data before LE↓	1.1		0.4		1.1		0.4		ns
t_H	Hold time, data after LE↓	1.7		2		1.4		1.4		ns

switching characteristics over recommended free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH373				SN74LVTH373				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
t _{PLH}	D	Q	1.4	4.1		4.7	1.5	2.6	3.9	4.5	ns
t _{PHL}			1.4	4.1		4.7	1.5	2.6	3.9	4.5	
t _{PLH}	LE	Q	1.6	4.4		5.1	1.7	2.7	4.2	4.9	ns
t _{PHL}			1.6	4.4		5.1	1.7	2.7	4.2	4.9	
t _{PZH}	OE	Q	1.2	5		6.1	1.3	3	4.8	5.9	ns
t _{PZL}			1.2	5		5.7	1.3	3	4.8	5.5	
t _{PHZ}	OE	Q	1.8	4.8		5.1	1.9	3	4.6	4.9	ns
t _{PLZ}			1.8	4.8		4.9	1.9	3	4.5	4.6	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



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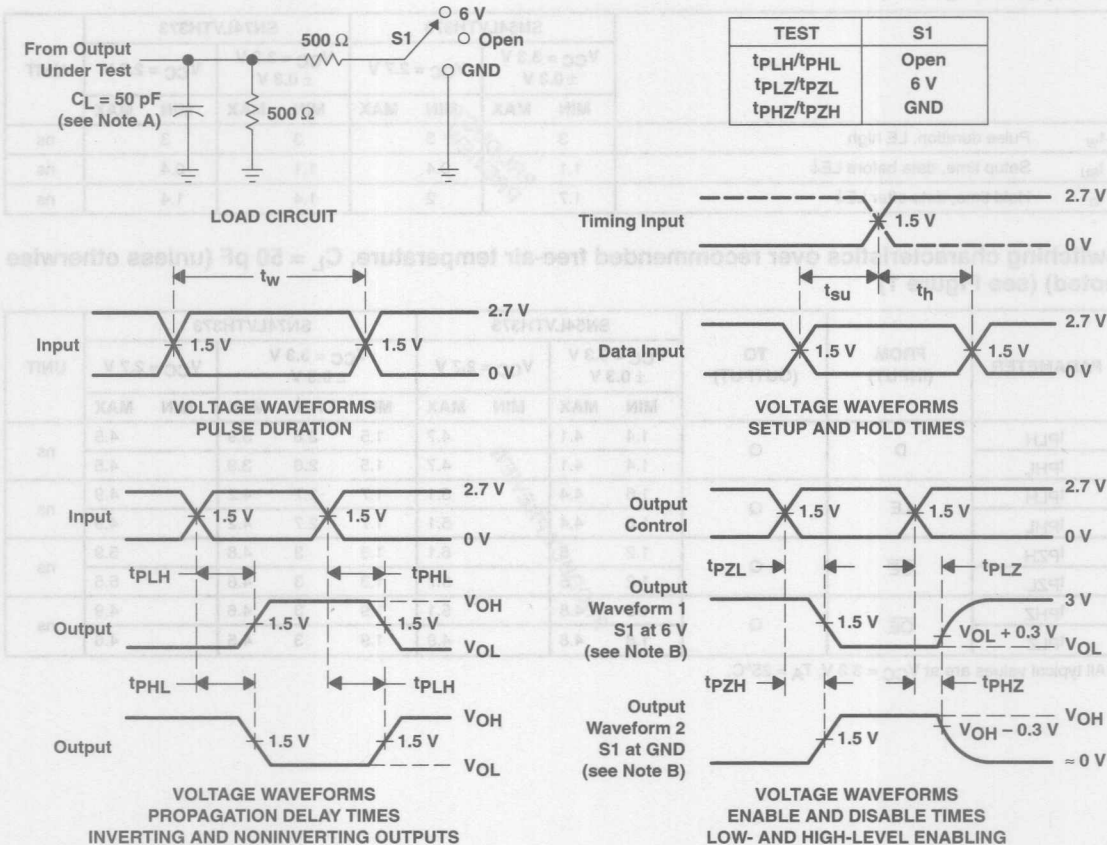


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SN54LVTH373, SN74LVTH373 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

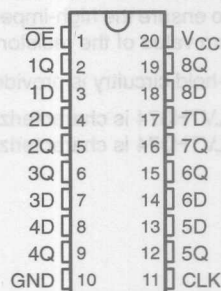
SN54LVTH374, SN74LVTH374

3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

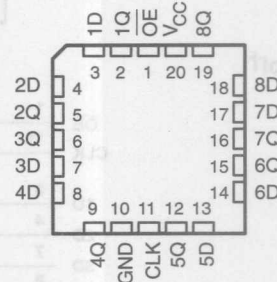
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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH374 ... J OR W PACKAGE
SN74LVTH374 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH374 ... FK PACKAGE
(TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVTH374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

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SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

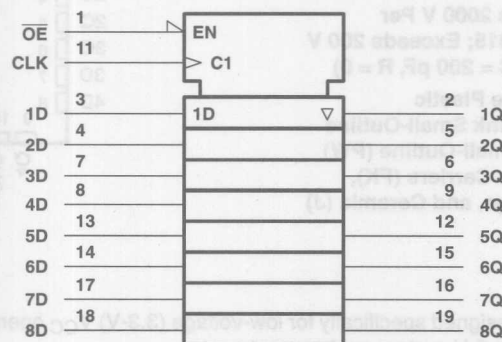
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH374 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

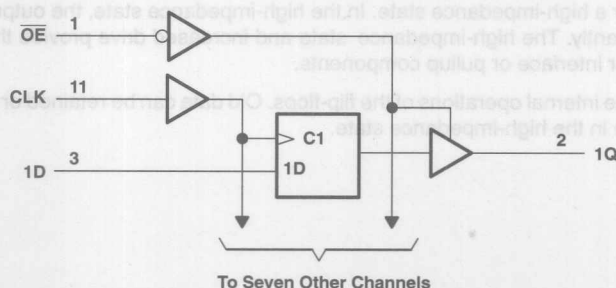
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



**TEXAS
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SN54LVTH374, SN74LVTH374

3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH374	96 mA
SN74LVTH374	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH374	48 mA
SN74LVTH374	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 4)

		SN54LVTH374		SN74LVTH374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH374, SN74LVTH374
3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

SCBS683D – MARCH 1997 – REVISED MARCH 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH374			SN74LVTH374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$			0.2			0.2	V
				0.5			0.5	
	$V_{CC} = 3 \text{ V}$			0.4			0.4	
				0.5			0.5	
				0.55			0.55	
				0.55			0.55	
I_I	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		10			10	μA
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$		1			1	
		$V_{CC} = 3.6 \text{ V}$, $V_I = 0$		-5			-5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75		75			μA
		$V_{CC} = 3 \text{ V}$, $V_I = 2 \text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$			3			3	pF
C_o	$V_O = 3 \text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPSWITH 3-STATE OUTPUTS

SCBS683D – MARCH 1997 – REVISED MARCH 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

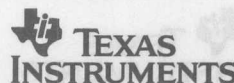
		SN54LVTH374				SN74LVTH374				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150		150		150		150		MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	1.6		2		1.5		2		ns
t_h	Hold time, data after CLK↑	0.8		0.5		0.8		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH374				SN74LVTH374				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150			150		MHz
t _{PLH}	CLK	Q	1.7	4.7	5.3		1.8	2.9	4.5	5		ns
t _{PHL}			1.7	4.5	4.6		1.8	2.9	4.2	4.3		
t _{PZH}	OE	Q	1.2	4.8	5.7		1.3	2.8	4.7	5.6		ns
t _{PZL}			1.5	4.8	5.4		1.6	3	4.7	5.2		
t _{PHZ}	OE	Q	1.8	4.8	5		1.9	3	4.6	4.9		ns
t _{PLZ}			1.9	4.9	5		2	3.1	4.5	4.6		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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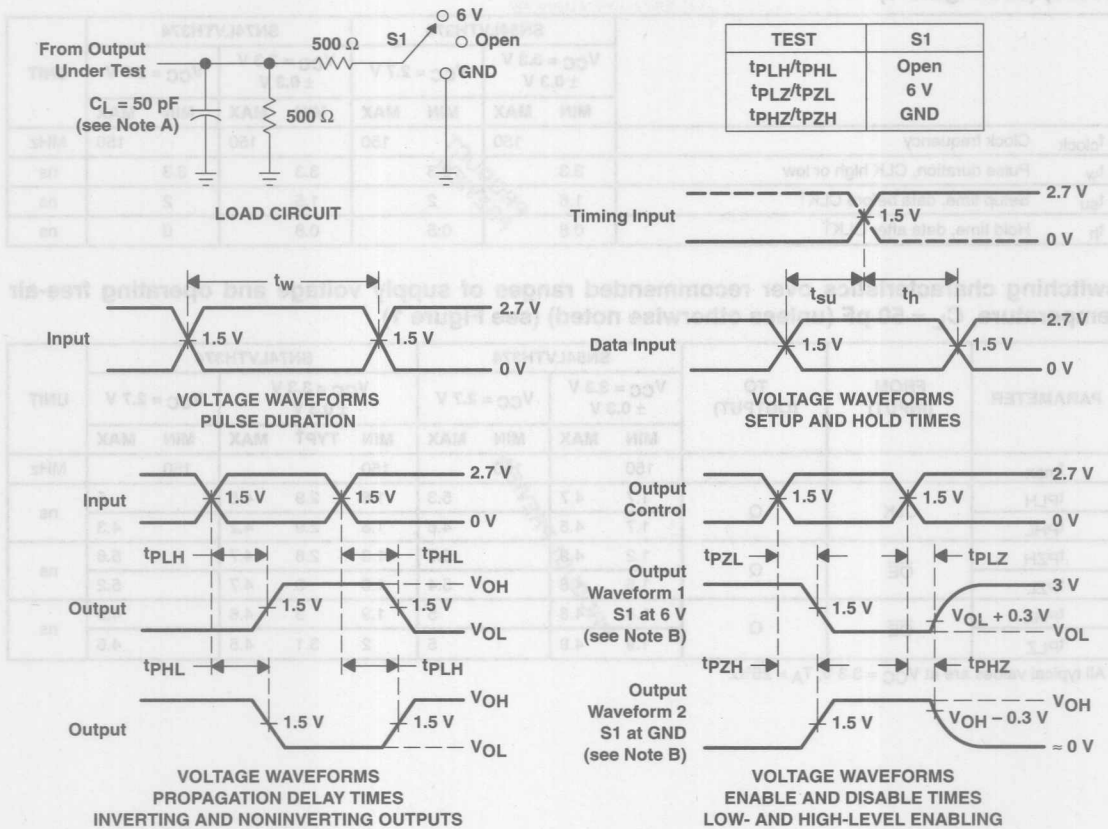


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SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS683D – MARCH 1997 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

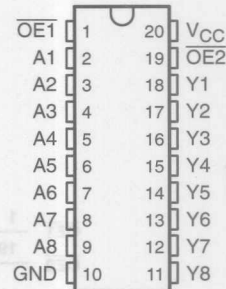
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

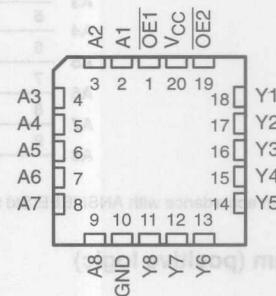
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- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH540 ... J OR W PACKAGE
SN74LVTH540 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH540 ... FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH540 devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH540 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH540 is characterized for operation from -40°C to 85°C .

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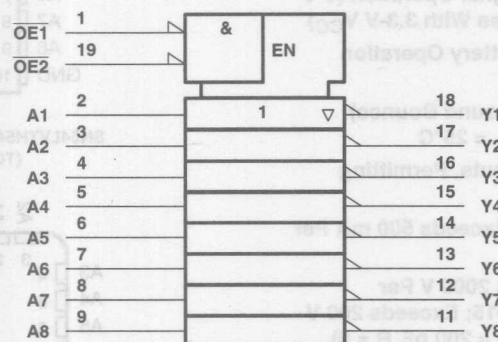
SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE

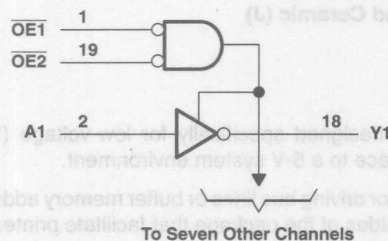
INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH540	96 mA
SN74LVTH540	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH540	48 mA
SN74LVTH540	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH540		SN74LVTH540		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200	μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH540, SN74LVTH540 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH540			SN74LVTH540			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			V
	$V_{CC} = 3\text{ V}$		2					V
					2			V
V_{OL}	$V_{CC} = 2.7\text{ V}$			0.2			0.2	V
				0.5			0.5	V
	$V_{CC} = 3\text{ V}$			0.4			0.4	V
				0.5			0.5	V
				0.55				V
							0.55	V
I_I	Control inputs	$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	μA
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	μA
	Data inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		1			1	μA
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		-5			-5	μA
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			μA
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	mA
		Outputs disabled		0.19			0.19	mA
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			3			3	pF
C_o	$V_O = 3\text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH540				SN74LVTH540				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1	3.9		4.7	1.1	2.4	3.8	4.6	ns	
t _{PHL}			1	3.9		4.7	1.1	2.7	3.8	4.6		
t _{PZH}	OE1 or OE2	Y	1.4	5.3		6.3	1.5	3.4	5.2	6.2	ns	
t _{PZL}			1.4	5.5		6.1	1.5	3.7	5.3	5.9		
t _{PHZ}	OE1 or OE2	Y	1.4	5.9		6.2	1.5	3.9	5.6	5.9	ns	
t _{PLZ}			1.4	5.5		5.8	1.5	3.5	5	5.3		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.



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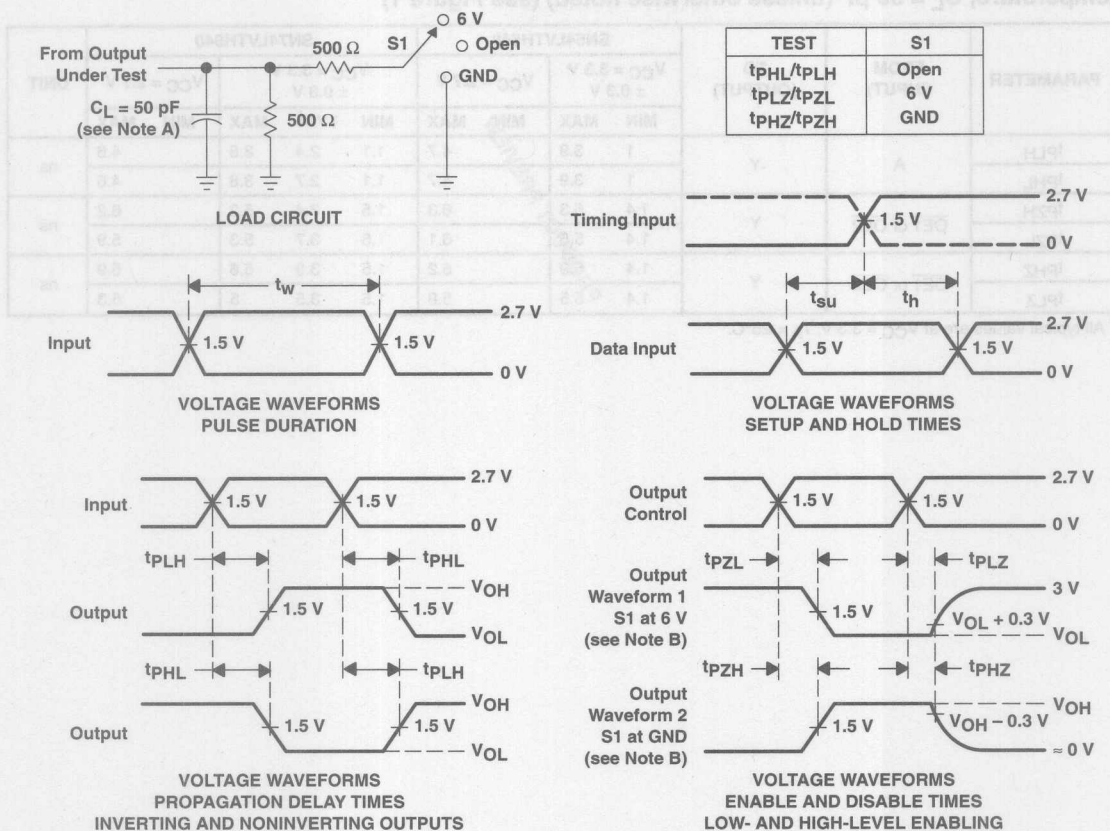
SN54LVTH540, SN74LVTH540

3.3-V ABT OCTAL BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS681D – MARCH 1997 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



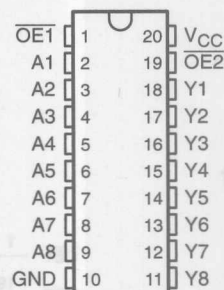
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SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

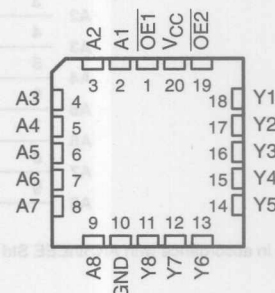
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH541 ... J OR W PACKAGE
SN74LVTH541 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH541 ... FK PACKAGE
(TOP VIEW)



description

These octal buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH541 devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH541 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH541 is characterized for operation from -40°C to 85°C .

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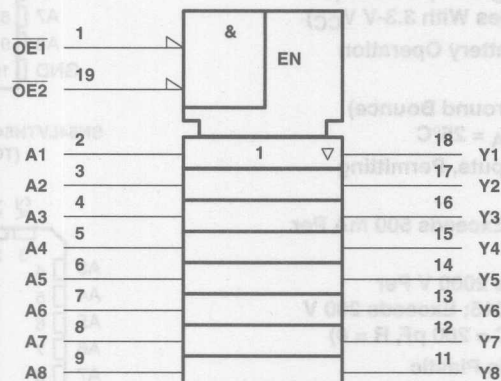
SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS682D – MARCH 1997 – REVISED MARCH 1998

FUNCTION TABLE

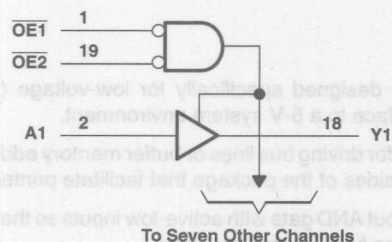
INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH541	96 mA
SN74LVTH541	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH541	48 mA
SN74LVTH541	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 4)

		SN54LVTH541		SN74LVTH541		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH541, SN74LVTH541
3.3-V ABT OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

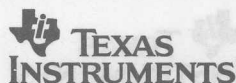
PARAMETER	TEST CONDITIONS	SN54LVTH541			SN74LVTH541			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7\text{ V}$			0.2			0.2	V
				0.5			0.5	
				0.4			0.4	
	$V_{CC} = 3\text{ V}$			0.5			0.5	
				0.55			0.55	
				0.55			0.55	
I_I	Control inputs	$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	μA
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		1			1	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		-5			-5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			3			3	pF
C_o	$V_O = 3\text{ V or } 0$			7			7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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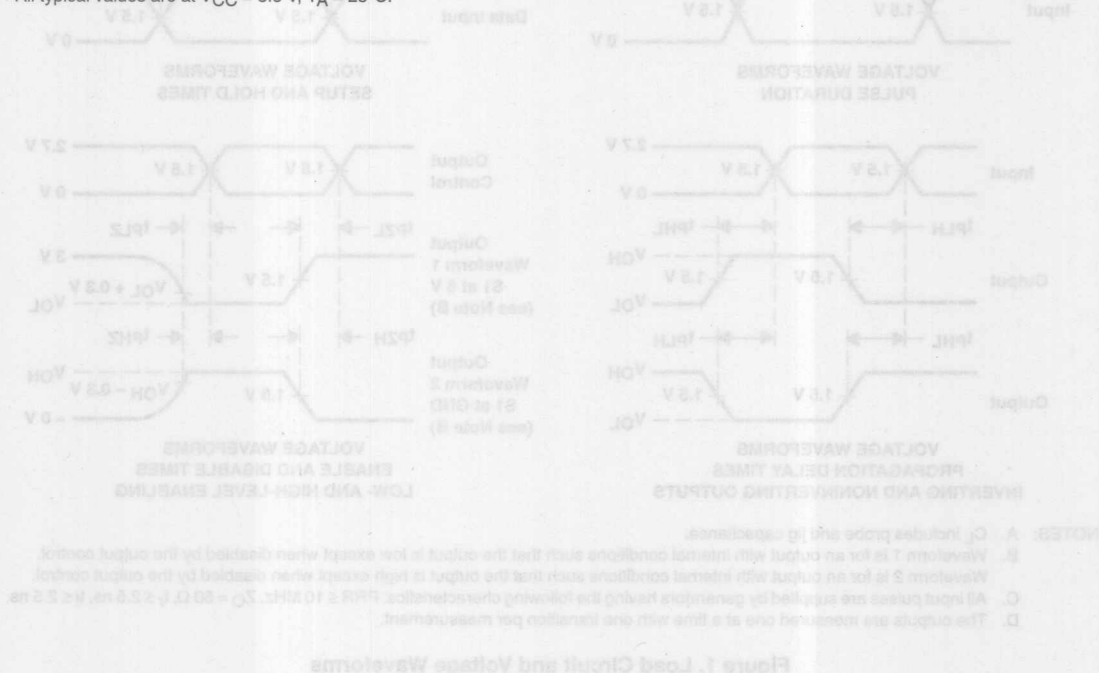
SN54LVTH541, SN74LVTH541 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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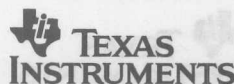
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH541				SN74LVTH541				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t_{PLH}	A	Y	1	3.7		4	1.1	2.4	3.5		3.9	ns
t_{PHL}			1	3.7		4	1.1	2.4	3.5		3.9	
t_{PZH}	$\overline{OE1}$ or $\overline{OE2}$	Y	1.4	5.3		6.3	1.5	3.5	5.2		6.2	ns
t_{PZL}			1.4	5.4		6	1.5	3.7	5.3		5.9	
t_{PHZ}	$\overline{OE1}$ or $\overline{OE2}$	Y	1.4	5.8		6.1	1.5	3.9	5.6		5.9	ns
t_{PLZ}			1.4	5.4		5.7	1.5	3	5		5.3	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.



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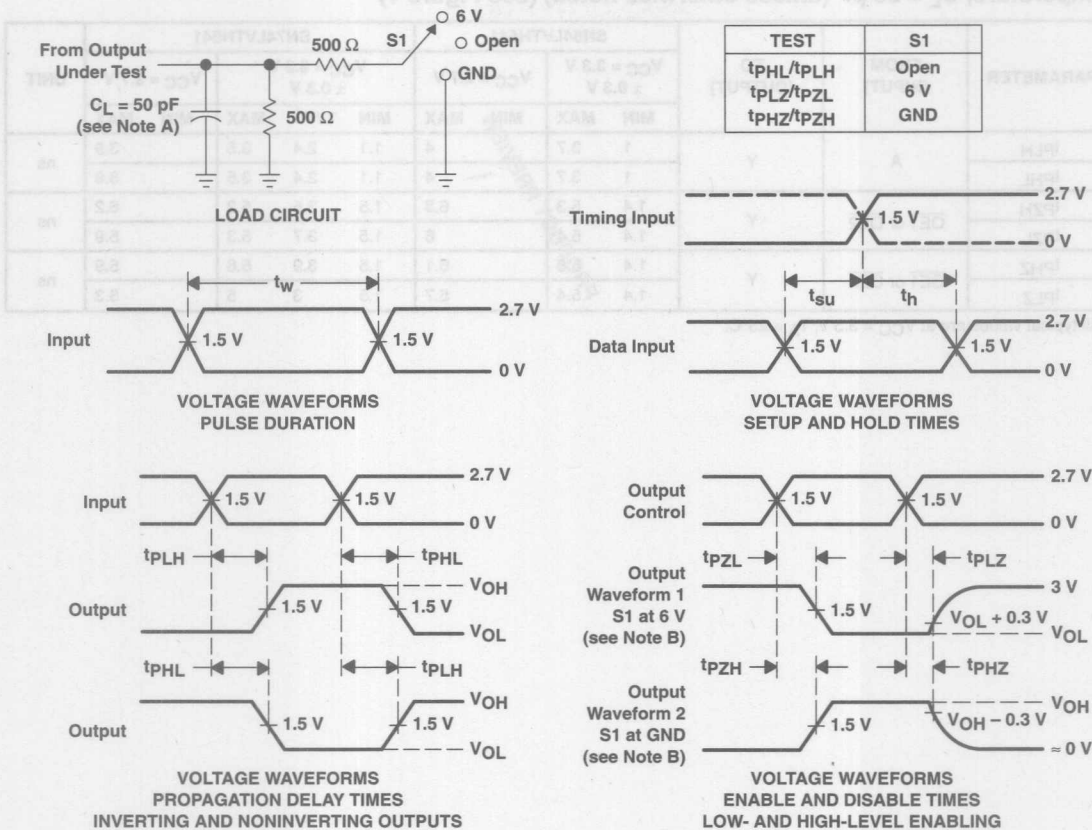


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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

description

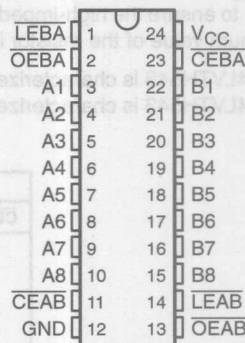
These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH543 devices contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

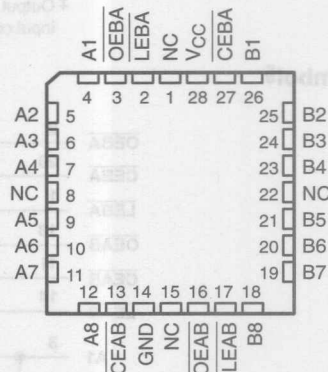
The A-to-B enable (\overline{CEAB}) input must be low to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54LVTH543 ... JT OR W PACKAGE
SN74LVTH543 ... DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH543 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54LVTH543, SN74LVTH543 **3.3-V ABT OCTAL REGISTERED TRANSCEIVERS** **WITH 3-STATE OUTPUTS**

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH543 is characterized for operation from -40°C to 85°C .

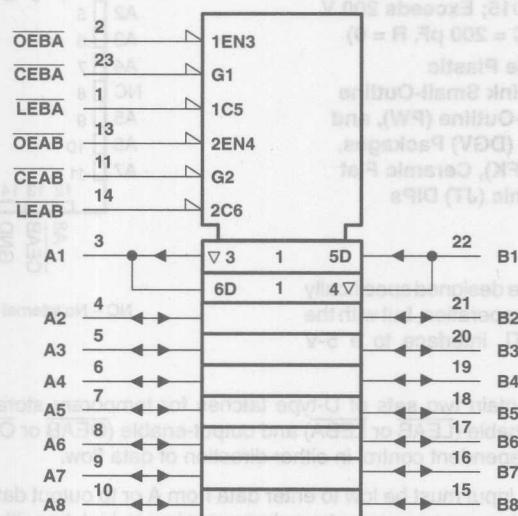
FUNCTION TABLE†

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^{\ddagger}
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

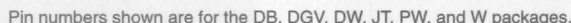
‡ Output level before the indicated steady-state input conditions were established

logic symbols



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

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Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH543	96 mA
SN74LVTH543	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH543	48 mA
SN74LVTH543	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

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recommended operating conditions (see Note 4)

		SN54LVTH543		SN74LVTH543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH543, SN74LVTH543
3.3-V ABT OCTAL REGISTERED TRANSCEIVERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH543			SN74LVTH543			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \text{ } \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
		$V_{CC} = 3 \text{ V}$, $I_{OH} = -32 \text{ mA}$	2			2			
V_{OL}		$V_{CC} = 2.7 \text{ V}$			0.2			0.2	V
					0.5			0.5	
		$V_{CC} = 3 \text{ V}$			0.4			0.4	
					0.5			0.5	
					0.55			0.55	
					0.55			0.55	
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$			± 1			± 1	μA
		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			10			10	
	A or B ports‡	$V_{CC} = 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			20			20	
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ $V_I = 0$			1 -5			1 -5	
I_{off}		$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_{I(\text{hold})}$	A or B ports	$V_{CC} = 3 \text{ V}$			75			75	μA
					-75			-75	
I_{OZPU}		$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}		$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$			0.19			0.19	mA
					5			5	
					0.19			0.19	
ΔI_{CC}^\S		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i		$V_I = 3 \text{ V or } 0$			4			4	pF
C_{io}		$V_O = 3 \text{ V or } 0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at V_{CC} or GND

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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 **TEXAS
INSTRUMENTS**

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SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVTH543				SN74LVTH543				UNIT
				V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration,	LEAB or LEBA low		3.3		3.3		3.3		3.3		ns
t _{su}	Setup time	A or B before LEAB or LEBA↑	Data high	0.4		0.4		0.4		0.4		ns
			Data low	1		1.5		1		1.5		
		A or B before CEAB or CEBA↑	Data high	0.2		0.2		0.2		0.2		
			Data low	0.7		1.2		0.7		1.2		
t _h	Hold time	A or B after LEAB or LEBA↑	Data high	1.5		0.6		1.5		0.6		ns
			Data low	1.3		1.5		1.3		1.5		
		A or B after CEAB or CEBA↑	Data high	1.6		0.5		1.6		0.5		
			Data low	1.4		1.6		1.4		1.6		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH543				SN74LVTH543				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A or B	B or A	1.2	3.9		4.5	1.3	2.5	3.7		4.3	ns
t _{PHL}			1.2	3.9		4.5	1.3	2.5	3.7		4.3	
t _{PLH}	LE	A or B	1.2	5.1		6.1	1.3	2.9	4.7		5.9	ns
t _{PHL}			1.2	5.1		6.1	1.3	2.9	4.7		5.9	
t _{PZH}	OE	A or B	1	5.1		6.4	1.1	2.9	4.9		6.2	ns
t _{PZL}			1	5.1		6.4	1.1	3.2	4.9		6.2	
t _{PHZ}	OE	A or B	1.9	5.6		6.2	2	3.4	5.3		5.9	ns
t _{PLZ}			1.9	5.6		6.2	2	3.7	5.3		5.9	
t _{PZH}	CE	A or B	1.2	5.5		7	1.3	3.2	5.3		6.8	ns
t _{PZL}			1.2	5.5		7	1.3	3.5	5.3		6.8	
t _{PHZ}	CE	A or B	2.2	5.7		6.2	2.3	3.8	5.4		5.9	ns
t _{PLZ}			2.2	5.7		5.9	2.3	3.9	5.4		5.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

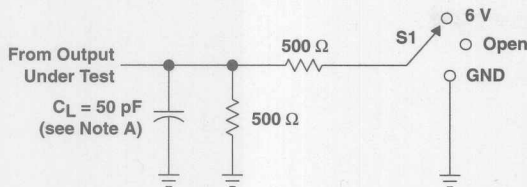


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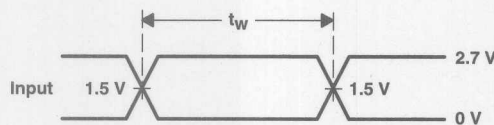
SN54LVTH543, SN74LVTH543 3.3-V ABT OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS704C – AUGUST 1997 – REVISED APRIL 1998

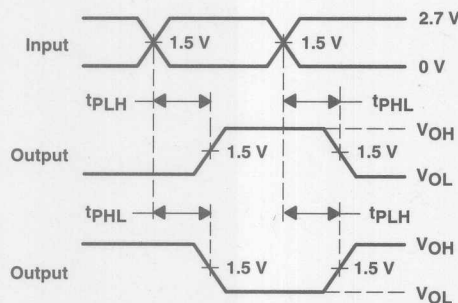
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

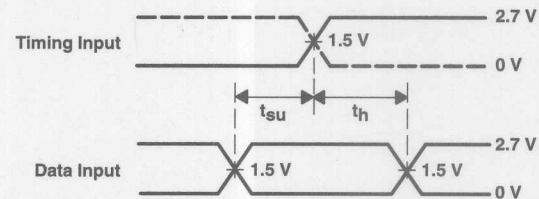


VOLTAGE WAVEFORMS
PULSE DURATION

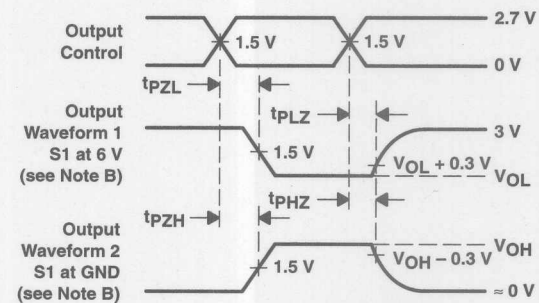


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



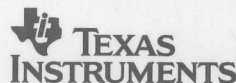
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION

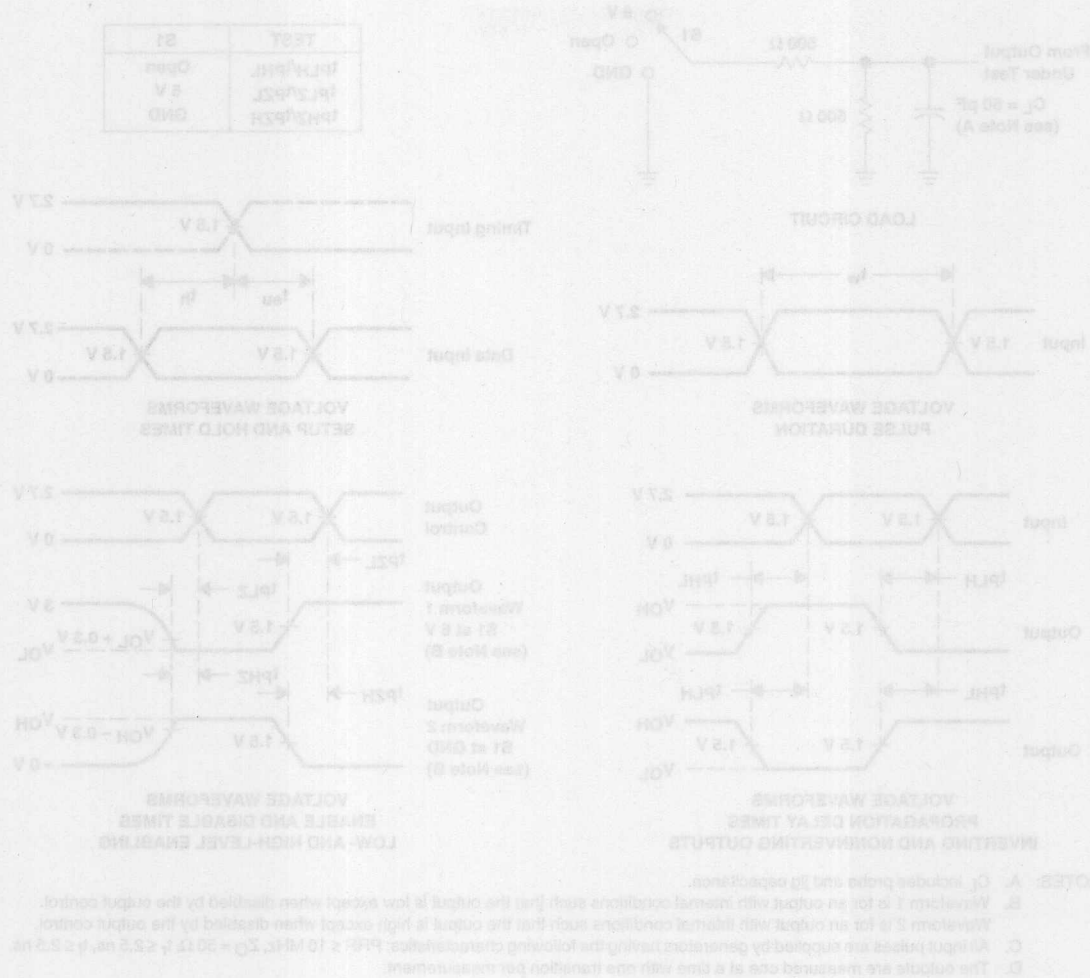


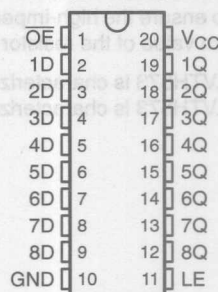
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

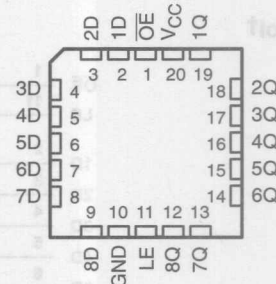
SCBS687D - MAY 1997 - REVISED APRIL 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH573 ... J OR W PACKAGE
SN74LVTH573 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH573 ... FK PACKAGE
(TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVTH573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS687D – MAY 1997 – REVISED APRIL 1998

description (continued)

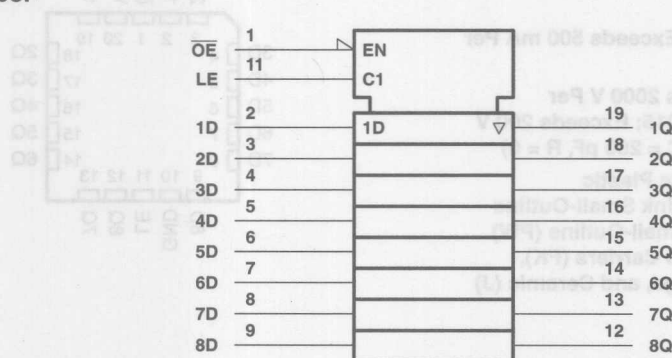
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH573 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH573 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each latch)

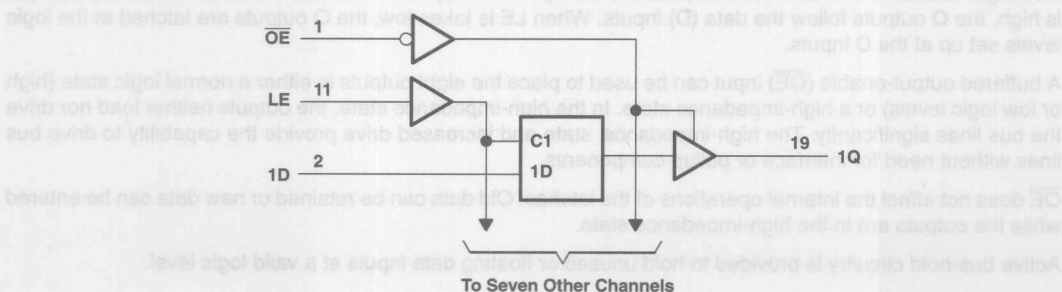
INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SN54LVTH573, SN74LVTH573 **3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS**

SCBS687D – MAY 1997 – REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH573	96 mA
SN74LVTH573	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH573	48 mA
SN74LVTH573	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH573		SN74LVTH573		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH573, SN74LVTH573
3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS687D – MAY 1997 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH573			SN74LVTH573			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$ $I_{OH} = -32 \text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$		0.5			0.5	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4			0.4	
		$I_{OL} = 32 \text{ mA}$		0.5			0.5	
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$					0.55	
I_I	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, Control inputs	$V_I = 5.5 \text{ V}$		10			10	μA
	$V_{CC} = 3.6 \text{ V}$, Data inputs	$V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	$V_{CC} = 3.6 \text{ V}$	$V_I = V_{CC}$		1			1	
		$V_I = 0$		-5			-5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$		75			75	μA
		$V_I = 2 \text{ V}$		-75			-75	
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$			3			3	pF
C_o	$V_O = 3 \text{ V or } 0$			7			7	pF

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS687D – MAY 1997 – REVISED APRIL 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH573				SN74LVTH573				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	3		3		3		3		ns
t_{SU}	Setup time, data before LE↓	0.7		0.6		0.7		0.6		ns
t_H	Hold time, data after LE↓	1.5		1.7		1.5		1.7		ns

switching characteristics over recommended free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

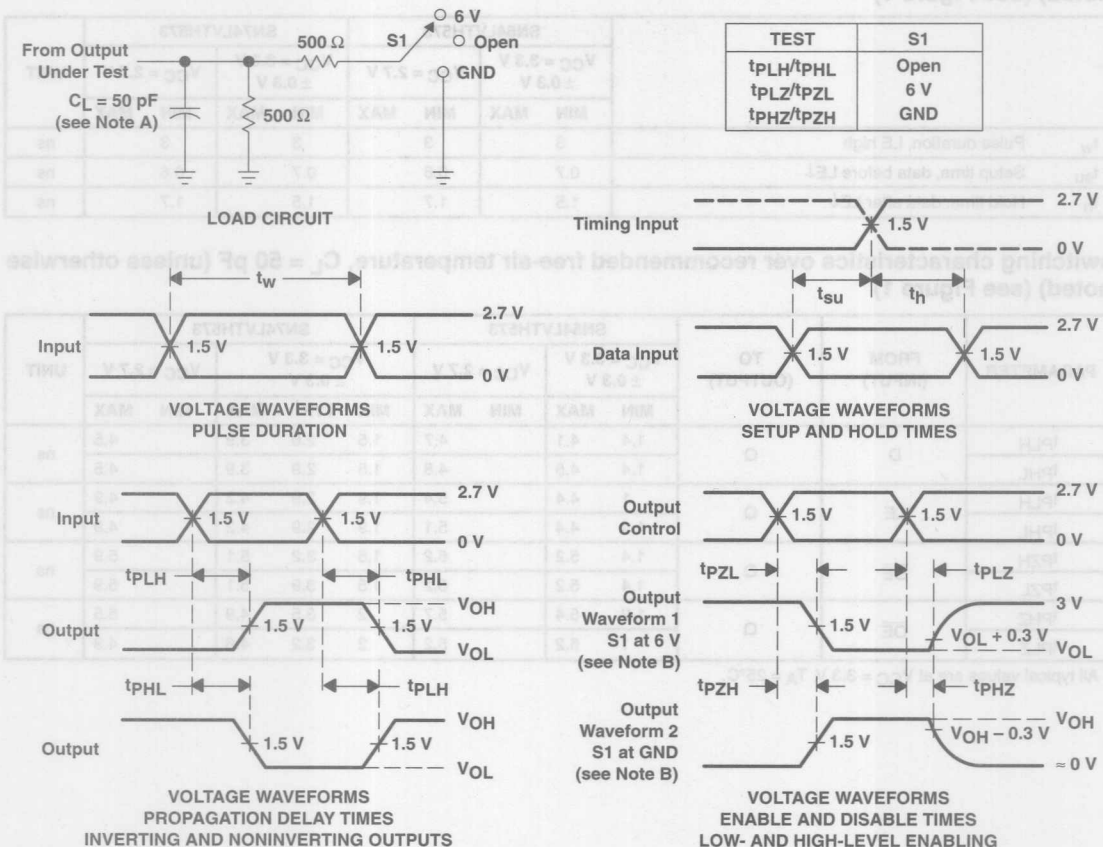
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH573				SN74LVTH573				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	D	Q	1.4	4.1		4.7	1.5	2.6	3.9		4.5	ns
t _{PHL}			1.4	4.5		4.8	1.5	2.9	3.9		4.5	
t _{PLH}	LE	Q	1	4.4		5.4	1.9	2.9	4.2		4.9	ns
t _{PHL}			1.4	4.4		5.1	1.9	2.9	4.2		4.9	
t _{PZH}	OE	Q	1.4	5.2		6.2	1.5	3.2	5.1		5.9	ns
t _{PZL}			1.4	5.2		6.2	1.5	3.9	5.1		5.9	
t _{PHZ}	OE	Q	1.2	5.4		5.7	2	3.5	4.9		5.5	ns
t _{PLZ}			1	5.2		5.2	2	3.2	4.6		4.9	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVTH573, SN74LVTH573 3.3-V ABT OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS687D – MAY 1997 – REVISED APRIL 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

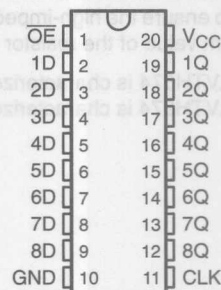
Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH574, SN74LVTH574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

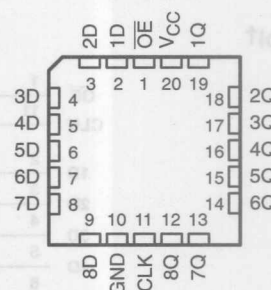
SCBS688C - MAY 1997 - REVISED MARCH 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (J) DIPs

SN54LVTH574 ... J OR W PACKAGE
SN74LVTH574 ... DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH574 ... FK PACKAGE
(TOP VIEW)



description

These octal flip-flops are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVTH574 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN54LVTH574, SN74LVTH574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS688C – MAY 1997 – REVISED MARCH 1998

description (continued)

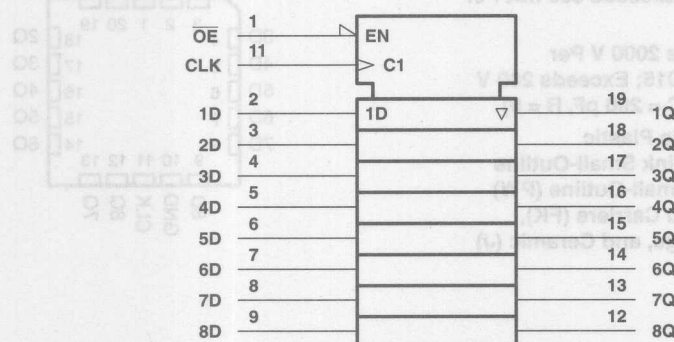
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH574 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH574 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

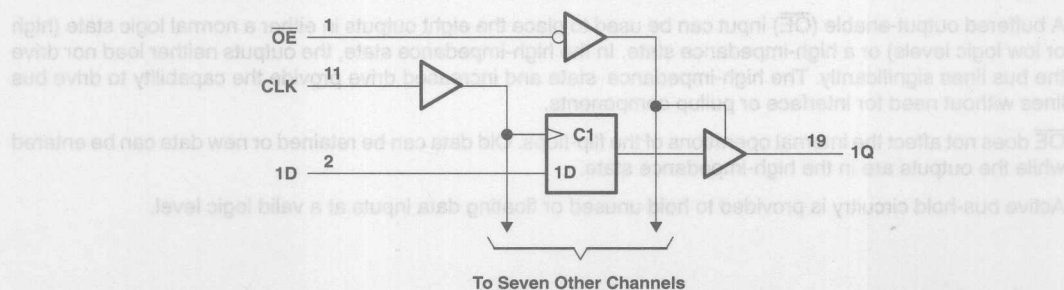
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SN54LVTH574, SN74LVTH574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS688C – MAY 1997 – REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH574	96 mA
SN74LVTH574	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH574	48 mA
SN74LVTH574	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	115°C/W
DW package	97°C/W
PW package	128°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH574		SN74LVTH574		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH574, SN74LVTH574
3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH574		SN74LVTH574		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2		-1.2	V
V _{OH}		V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2			V
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4			
		V _{CC} = 3 V	I _{OH} = -24 mA	2					
			I _{OH} = -32 mA				2		
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2		0.2	V
			I _{OL} = 24 mA			0.5		0.5	
		V _{CC} = 3 V	I _{OL} = 16 mA			0.4		0.4	
			I _{OL} = 32 mA			0.5		0.5	
			I _{OL} = 48 mA			0.55			
			I _{OL} = 64 mA				0.55		
I _I		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10		10	μA
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1		±1	
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}			1		1	
			V _I = 0			-5		-5	
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V					±100	μA
I _I (hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75			μA
			V _I = 2 V	-75		-75			
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5		5	μA
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			-5		-5	μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care					±100*	±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care					±100*	±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			0.19		0.19	mA
			Outputs low			5		5	
			Outputs disabled			0.19		0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND					0.2	0.2	mA
C _i		V _I = 3 V or 0					3	3	pF
C _o		V _O = 3 V or 0					7	7	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH574, SN74LVTH574 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH574				SN74LVTH574				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150		150		150		150		MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2		2.4		2		2.4		ns
t_h	Hold time, data after CLK↑	0.9		0.9		0.3		0		ns

switching characteristics over recommended free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH574				SN74LVTH574				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150		150		150			150		MHz
t_{PLH}	CLK	Q	1.7	4.9	5.9		1.8	3	4.5	5.3		ns
t_{PHL}			1.7	4.9	5.5		1.8	3	4.5	5.3		
t_{PZH}	$\overline{\text{OE}}$	Q	1.4	5.1	6.5		1.5	3.2	4.8	5.9		ns
t_{PZL}			1.4	5.1	6.1		1.5	3.5	4.8	5.9		
t_{PHZ}	$\overline{\text{OE}}$	Q	1	5.9	6.4		2	3.5	4.8	5.1		ns
t_{PLZ}			0.8	4.8	5.3		2	3.2	4.4	4.4		

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

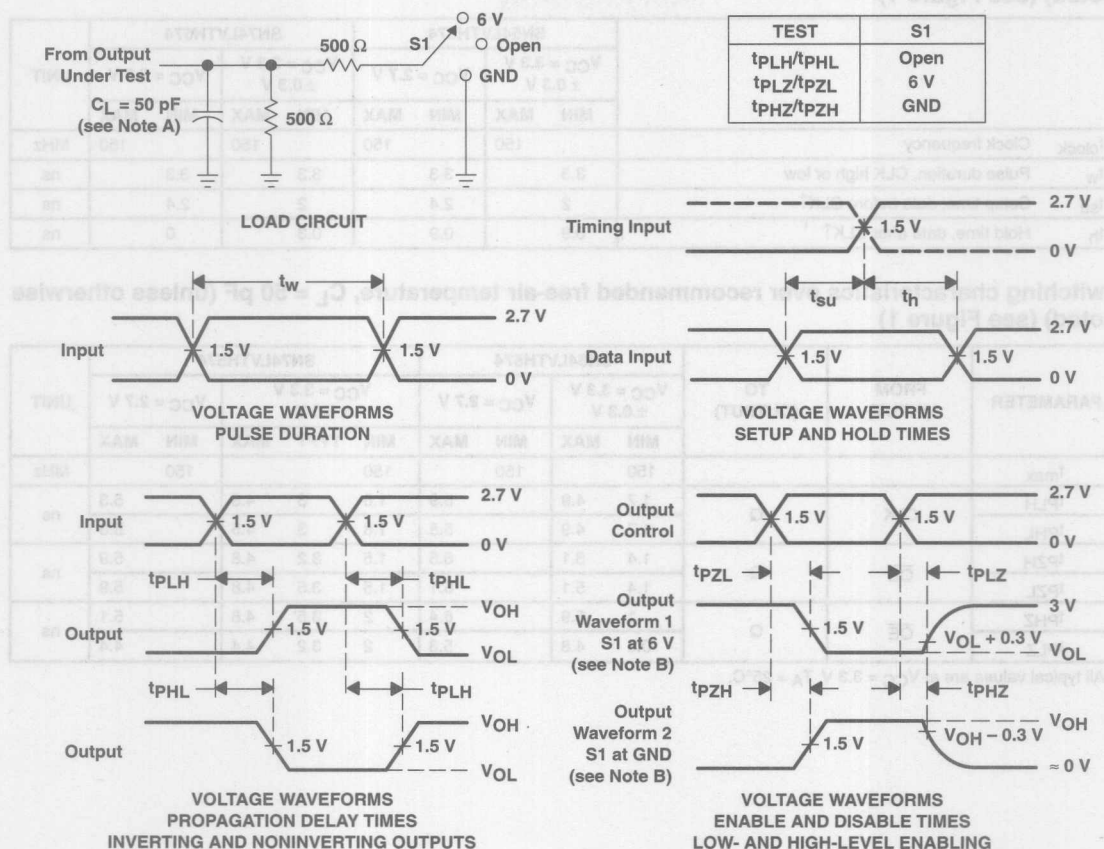
SN54LVTH574, SN74LVTH574

3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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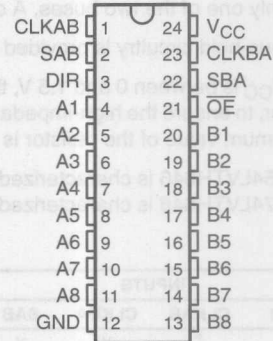
SN54LVTH646, SN74LVTH646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

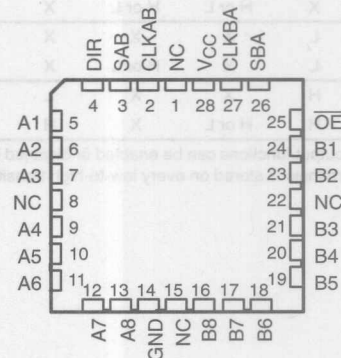
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

SN54LVTH646 . . . JT OR W PACKAGE
SN74LVTH646 . . . DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH646 devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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description (continued)

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH646 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH646 is characterized for operation from -40°C to 85°C .

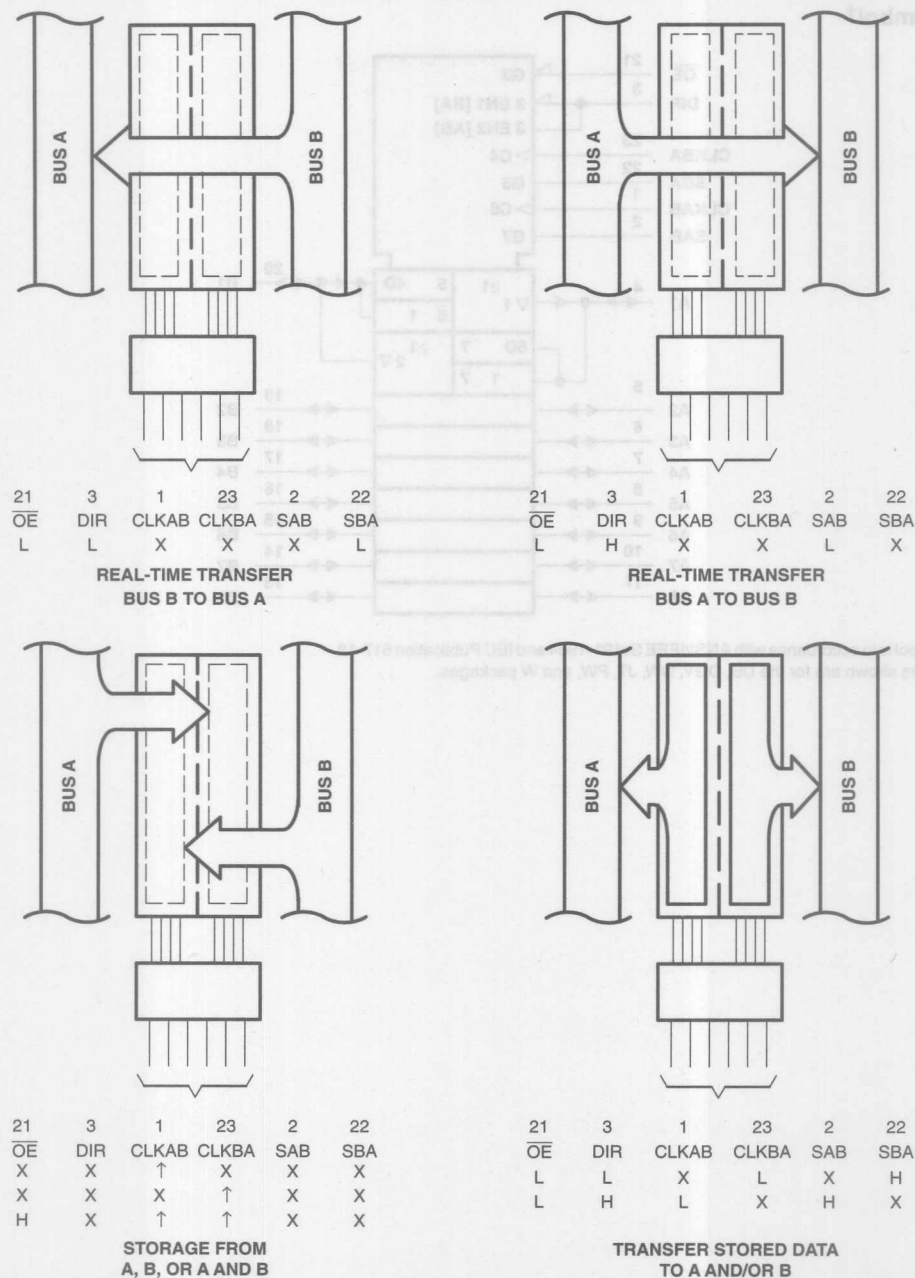
FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKA/B	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	\uparrow	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	\uparrow	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	\uparrow	\uparrow	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

[†] The data-output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

SN54LVTH646, SN74LVTH646
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

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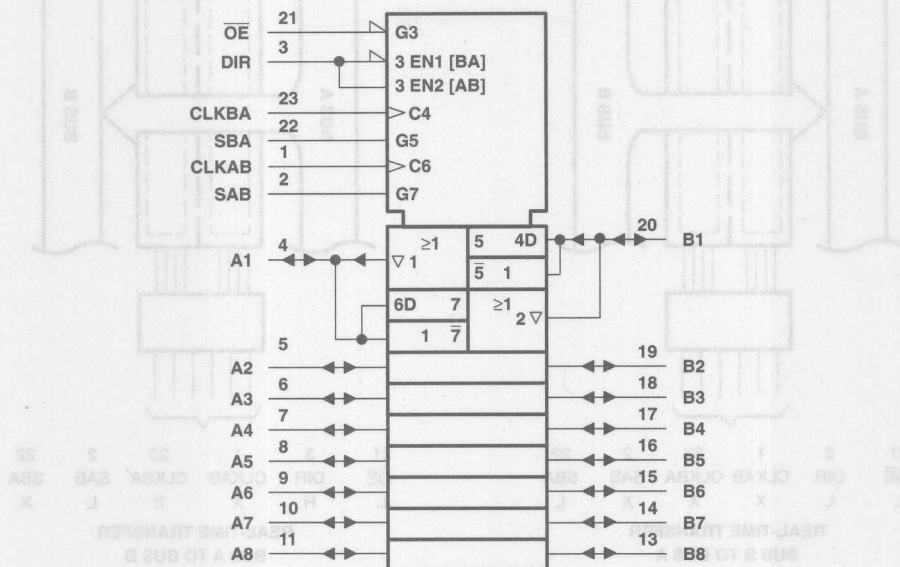
Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

Figure 1. Bus-Management Functions

SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic symbol†

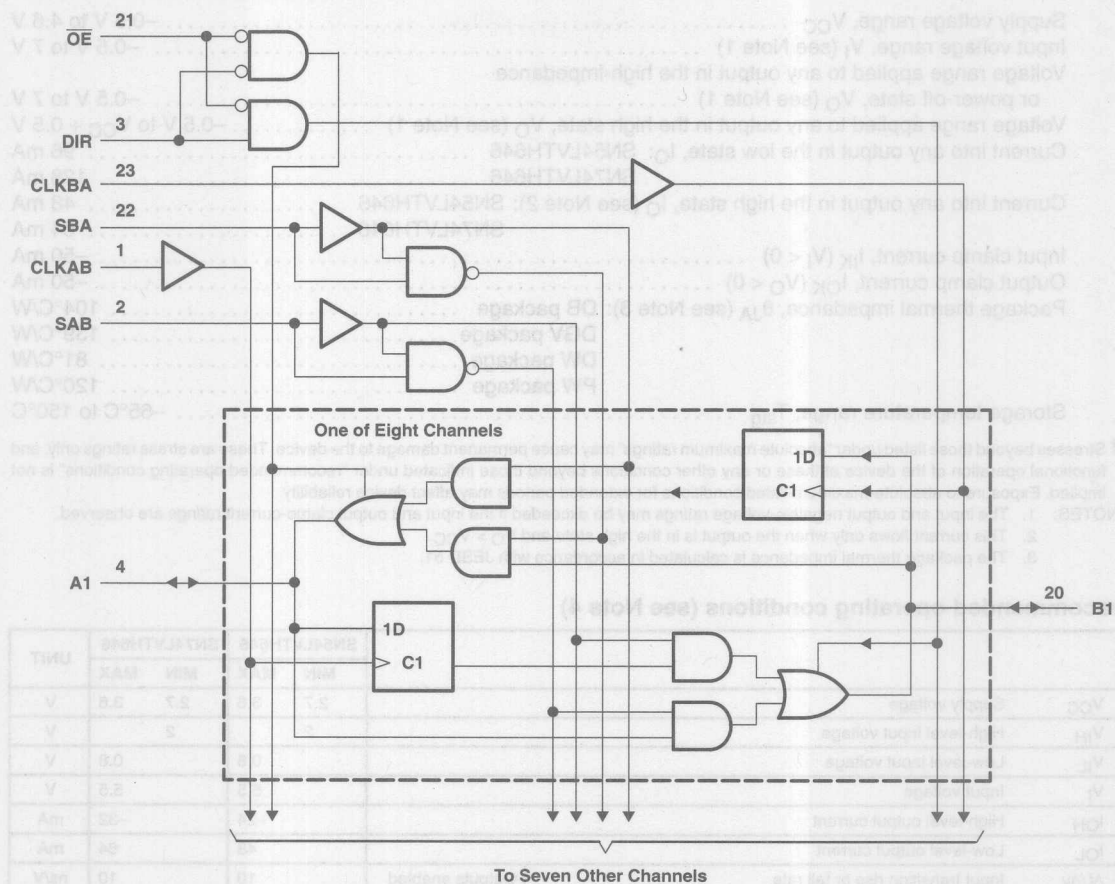


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

SN54LVTH646, SN74LVTH646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH646	96 mA
SN74LVTH646	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH646	48 mA
SN74LVTH646	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH646		SN74LVTH646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta V/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH646			SN74LVTH646			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$							
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
		$I_{OL} = 16\text{ mA}$		0.4			0.4	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$		0.55				
		$I_{OL} = 64\text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		20			20	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		1			1	
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$					± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$		$\pm 100^*$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$		$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\S		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2	mA
C_i		$V_I = 3\text{ V or } 0$		4			4	pF
C_{io}		$V_O = 3\text{ V or } 0$		9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at $V_{CC}\text{ or GND}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.



SN54LVTH646, SN74LVTH646 **3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS** **WITH 3-STATE OUTPUTS**

SCBS705C – AUGUST 1997 – REVISED APRIL 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

SYMBOL	SN54LVTH646		SN54LVTH646				SN74LVTH646				UNIT
	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V				
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
f _{clock}	Clock frequency		150		150		150		150		MHz
t _w	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑		Data high		1.3		1.6		1.2		ns
			Data low		1.9		2.6		1.6		
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑		1.2		1.2		0.8		0.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH646				SN74LVTH646				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150			150		MHz
t _{PLH}	CLKBA or CLKAB	A or B	1	5		5.9	1.8	3.1	4.7		5.6	ns
t _{PHL}			1.5	5		5.9	1.8	3.1	4.7		5.6	
t _{PLH}	A or B	B or A	1.1	4.9		5.6	1.3	2.3	3.5		4.1	ns
t _{PHL}			1.2	4.8		5	1.3	2.4	3.5		4.1	
t _{PLH}	SBA or SAB‡	A or B	1.1	5.3		6.3	1.5	3	4.9		6	ns
t _{PHL}			1.3	5.3		6.3	1.5	3.3	4.9		6	
t _{PZH}	$\overline{\text{OE}}$	A or B	1	5.4		6.7	1.1	3.1	5.2		6.5	ns
t _{PZL}			1	5.6		6.7	1.1	3.4	5.2		6.5	
t _{PHZ}	$\overline{\text{OE}}$	A or B	1.7	6		6.5	2.3	3.9	5.5		6.1	ns
t _{PLZ}			2.2	6.3		6.5	2.3	4	5.5		5.9	
t _{PZH}	DIR	A or B	1.2	5.6		6.8	1.3	3.4	5.2		6.6	ns
t _{PZL}			1.2	5.7		6.8	1.3	3.6	5.2		6.6	
t _{PHZ}	DIR	A or B	1.1	5.8		6.9	1.5	3.2	5.6		6.7	ns
t _{PLZ}			1.4	6.1		6.6	1.5	3.8	5.6		6.3	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

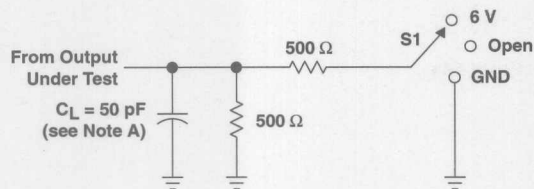
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.



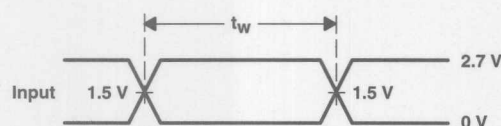
SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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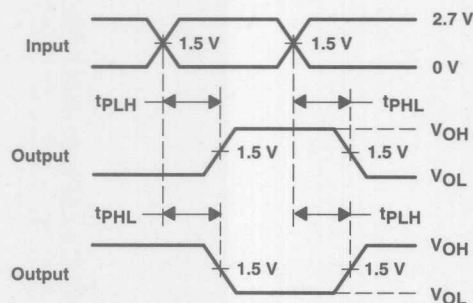
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

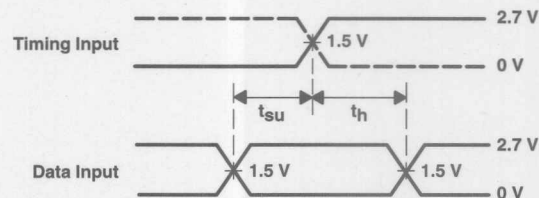


VOLTAGE WAVEFORMS
PULSE DURATION

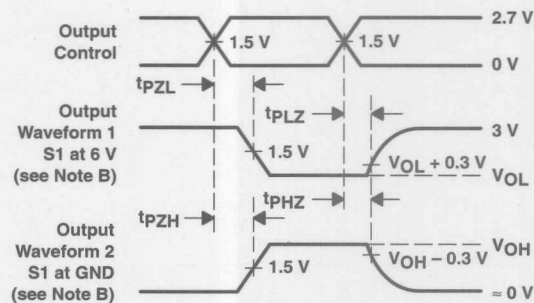


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION

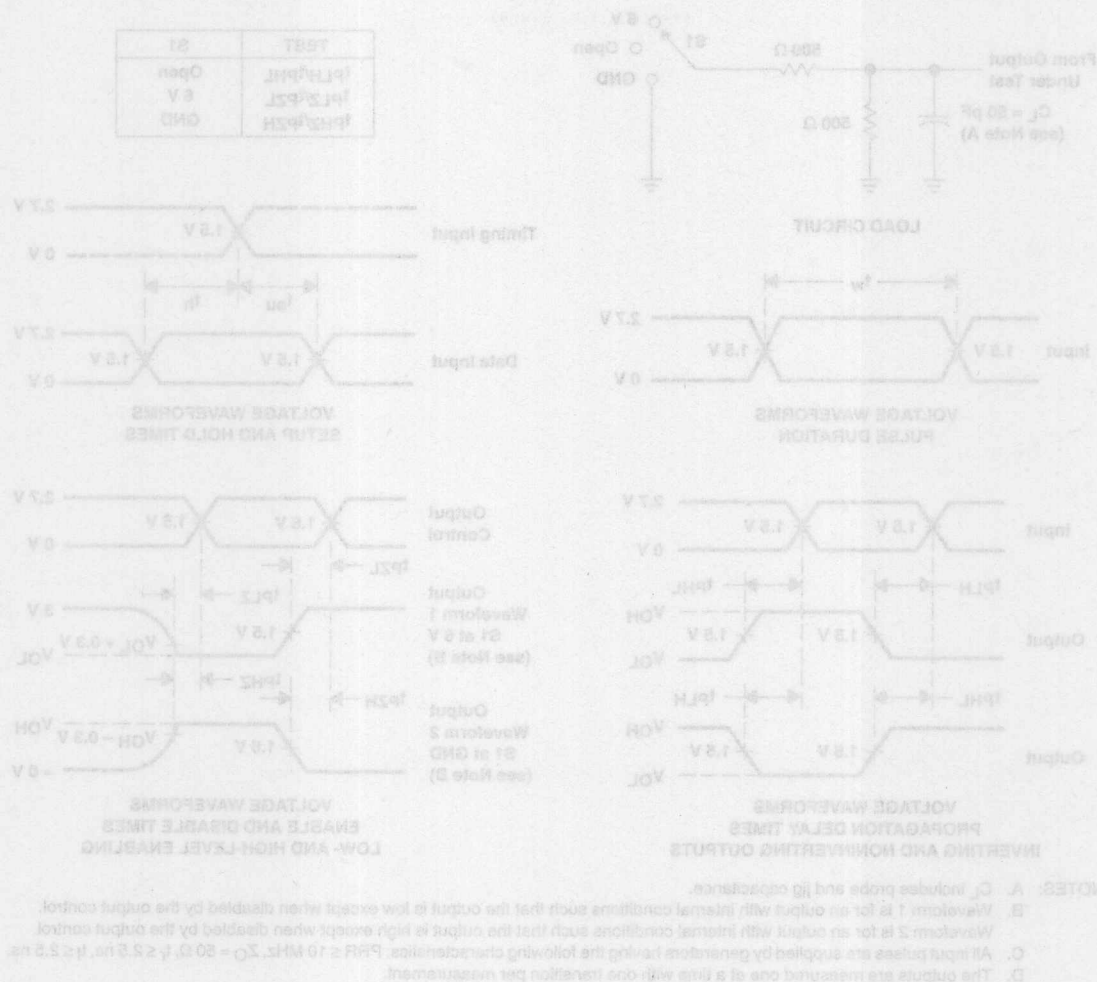


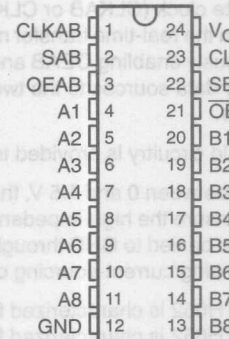
Figure 2. Load Circuit and Voltage Waveforms

SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

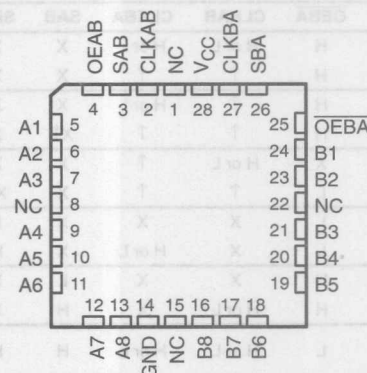
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Ceramic (JT) DIPs

SN54LVTH652 ... JT OR W PACKAGE
SN74LVTH652 ... DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH652 ... FK PACKAGE
(TOP VIEW)



description

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH652 devices.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN54LVTH652, SN74LVTH652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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description (continued)

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH652 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH652 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

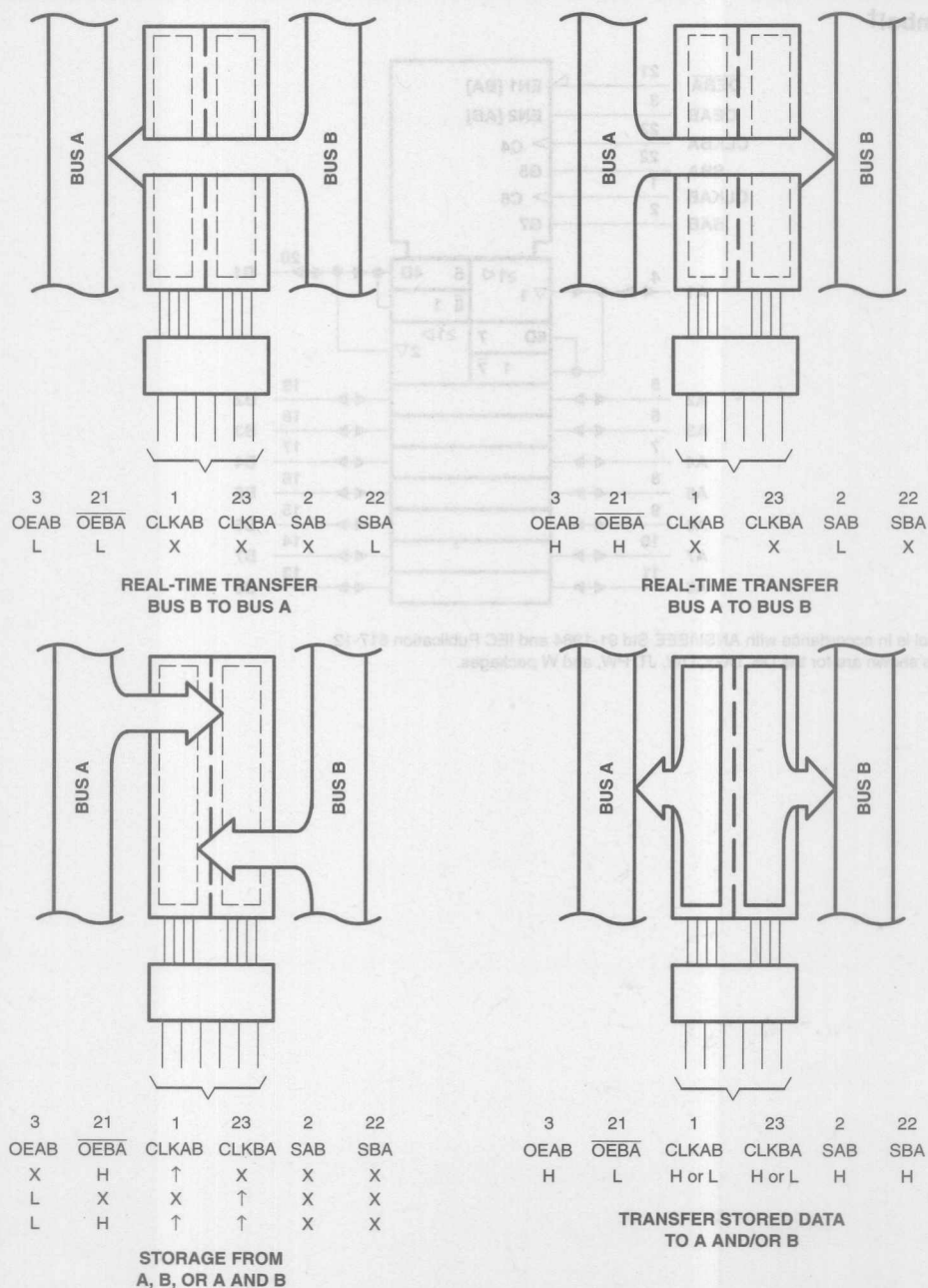
† The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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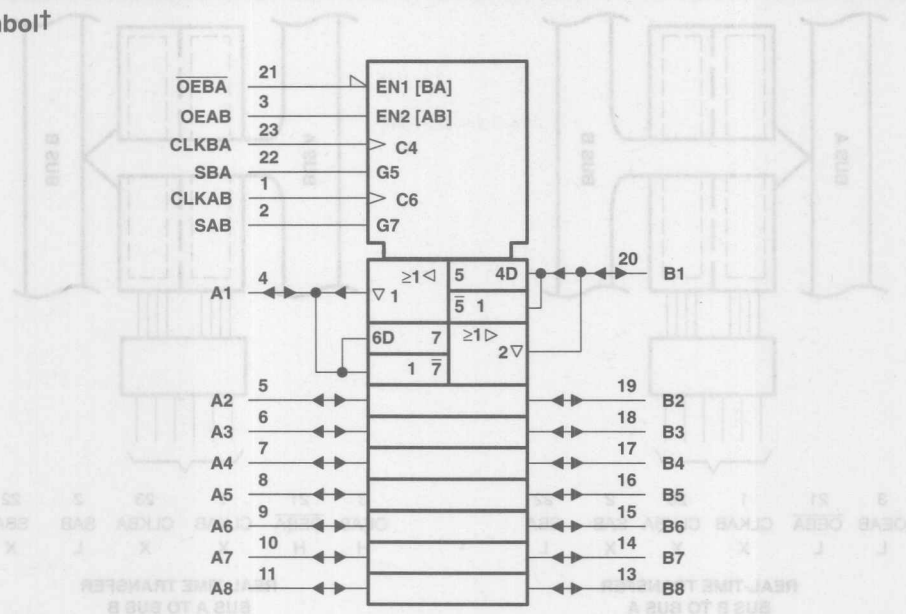
Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

Figure 1. Bus-Management Functions

SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic symbol†

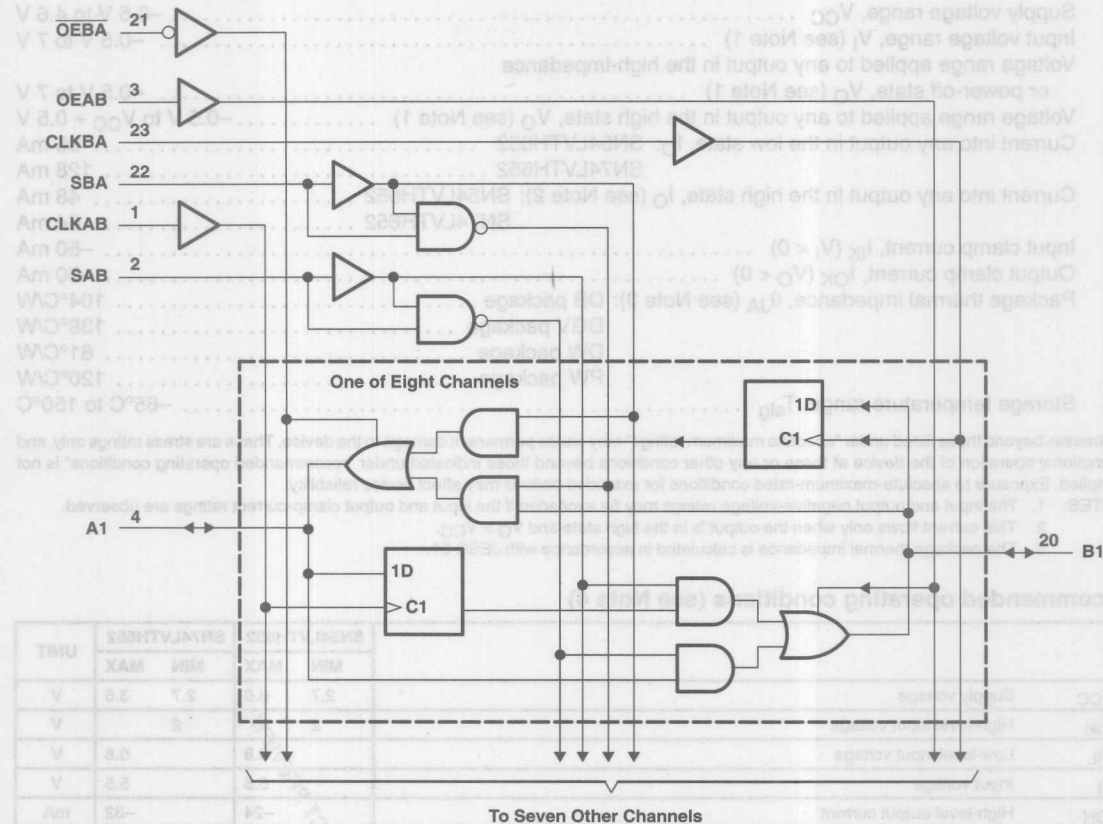


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, PW, and W packages.

UNIT	MIN	MAX	MIN	MAX
V	2.7	3.6	2.7	3.6
V	0.5	0.5	0.5	0.5
V	0.5	0.5	0.5	0.5
V	0.5	0.5	0.5	0.5
mA	-35	-35	-35	-35
ns	10	10	10	10
ns	200	200	200	200
°C	-55	125	-55	125

SN54LVTH652, SN74LVTH652

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH652	96 mA
SN74LVTH652	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH652	48 mA
SN74LVTH652	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH652		SN74LVTH652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH652			SN74LVTH652			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$							
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4			0.4	
		$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$		0.55			0.55	
		$I_{OL} = 64\text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		20			20	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		1			1	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ to } 3\text{ V}$, OE/OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ to } 3\text{ V}$, OE/OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^{\S}	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			4			4	pF
C_{io}	$V_O = 3\text{ V or } 0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at $V_{CC}\text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

TIME	SN74LVTH652		SN74LVTH652		SN54LVTH652				SN74LVTH652				UNIT
	MAX		MIN		MAX		MIN		MAX		MIN		
	V		2.7		2.7		3.3		3.3		3.3		
	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V						
	MIN		MAX		MIN		MAX		MIN		MAX		
f _{clock}	Clock frequency				150		150		150		150		MHz
t _w	Pulse duration, CLK high or low				3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑				1.3		1.6		1.2		1.5		ns
					1.9		2.6		1.6		2.2		
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑				1.2		1.2		0.8		0.8		ns

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH652				SN74LVTH652				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150		150		150			150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.7	5	5.9		1.8	3.1	4.7	5.6		ns
t_{PHL}			1.7	5	5.9		1.8	3.1	4.7	5.6		
t_{PLH}	A or B	B or A	1.2	3.7	4.3		1.3	2.3	3.5	4.1		ns
t_{PHL}			1.2	3.7	4.3		1.3	2.4	3.5	4.1		
t_{PLH}	SBA or SAB‡	A or B	1.4	5.2	6.3		1.5	3.1	4.9	6		ns
t_{PHL}			1.4	5.2	6.3		1.5	3.4	4.9	6		
t_{PZH}	$\overline{\text{OEBA}}$	A	1	5.4	6.7		1.1	2.9	5.2	6.5		ns
t_{PZL}			1	5.4	6.7		1.1	3.1	5.2	6.5		
t_{PHZ}	$\overline{\text{OEBA}}$	A	2.2	5.9	6.5		2.3	3.5	5.5	6.1		ns
t_{PLZ}			2.2	5.9	6.3		2.3	3.7	5.5	5.9		
t_{PZH}	OEAB	B	1.2	4.9	5.9		1.3	3	4.7	5.7		ns
t_{PZL}			1.2	4.9	5.9		1.3	3.3	4.7	5.7		
t_{PHZ}	OEAB	B	1.4	5.8	7		1.5	3.6	5.6	6.7		ns
t_{PLZ}			1.4	5.9	6.6		1.5	3.7	5.6	6.3		

\dagger All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

\ddagger These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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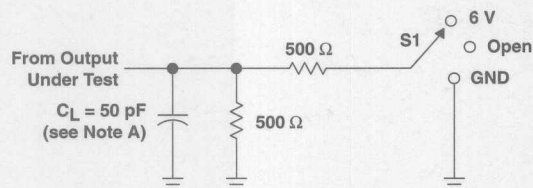


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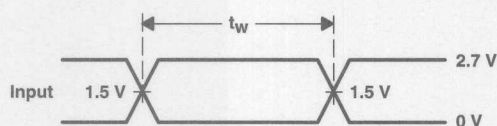
SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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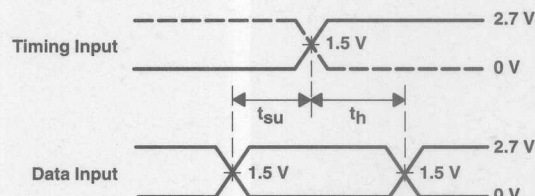
PARAMETER MEASUREMENT INFORMATION



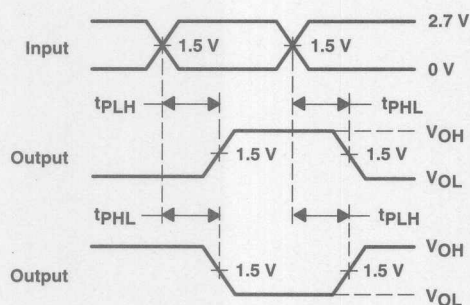
LOAD CIRCUIT



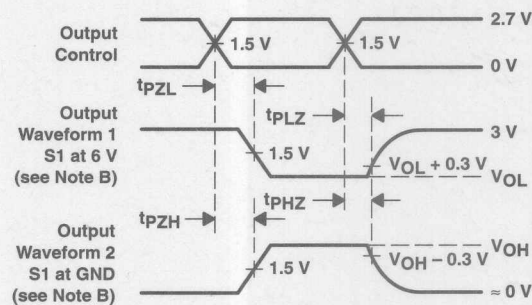
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

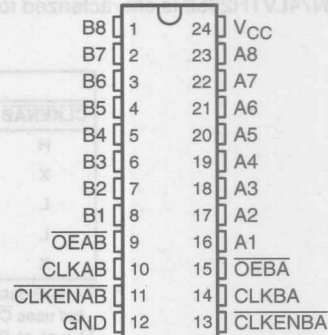


SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

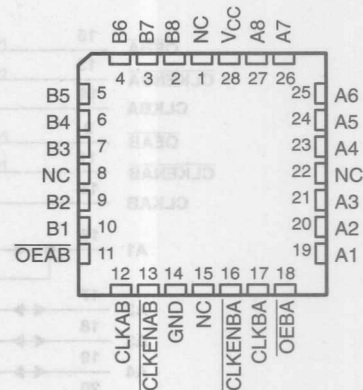
SCBS710C – OCTOBER 1997 – REVISED APRIL 1998

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

SN54LVTH2952 ... JT PACKAGE
SN74LVTH2952 ... DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH2952 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

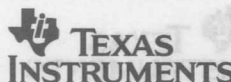
These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH2952 devices consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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SN54LVTH2952, SN74LVTH2952

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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description (continued)

The SN54LVTH2952 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74LVTH2952 is characterized for operation from -40°C to 85°C .

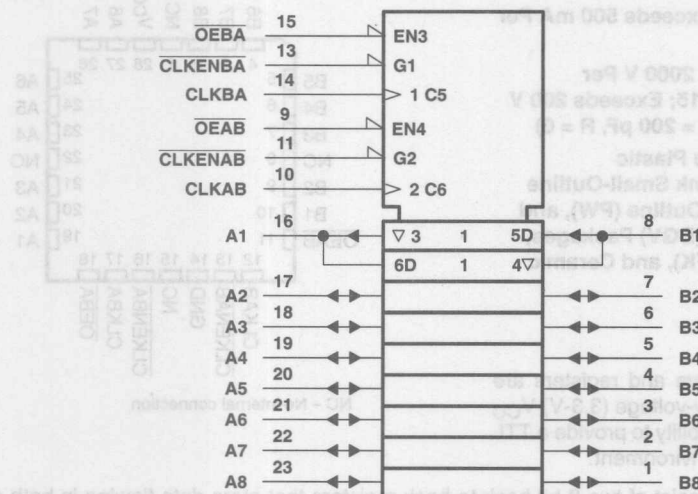
FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B_0^{\ddagger}
X	H or L	L	X	B_0^{\ddagger}
L	\uparrow	L	L	L
L	\uparrow	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

logic symbols



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DGV, DW, JT, and PW packages.

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Pin numbers shown are for the DB, DGV, DW, JT, and PW packages.

SN54LVTH2952, SN74LVTH2952

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH2952	96 mA
SN74LVTH2952	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH2952	48 mA
SN74LVTH2952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH2952		SN74LVTH2952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH2952, SN74LVTH2952

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH2952		SN74LVTH2952		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2		-1.2	V
V_{OH}		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$		V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4		
		$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2					
		$I_{OH} = -32\text{ mA}$					2		
V_{OL}		$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2		0.2	V
			$I_{OL} = 24\text{ mA}$			0.5		0.5	
			$I_{OL} = 16\text{ mA}$			0.4		0.4	
		$V_{CC} = 3\text{ V}$	$I_{OL} = 32\text{ mA}$			0.5		0.5	
			$I_{OL} = 48\text{ mA}$			0.55			
			$I_{OL} = 64\text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$				± 1		± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$				10		10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				20		20	
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ $V_I = 0$				1 -5		1 -5	
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75		75			μA
		$V_I = 2\text{ V}$		-75		-75			
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, OE = don't care				$\pm 100^*$		± 100	μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, OE = don't care				$\pm 100^*$		± 100	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high			0.19		0.19	mA
			Outputs low			5		5	
			Outputs disabled			0.19		0.19	
ΔI_{CC}^\S		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.2		0.2	mA
C_i		$V_I = 3\text{ V or } 0$				4		4	pF
C_{io}		$V_O = 3\text{ V or } 0$				9		9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at $V_{CC}\text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH2952				SN74LVTH2952				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency		150		150		150		150		MHz	
t _w	Pulse duration	CLK high	3.3		3.3		3.3		3.3		ns	
		CLK low	3.3		3.3		3.3		3.3			
t _{su}	Setup time	A or B before CLK↑	Data high	1.6		2.2		1.5		2.1		ns
			Data low	1.6		2.2		1.5		2.1		
		CE̅ before CLK↑	Data high	1.6		1.9		1.5		1.8		
			Data low	2		2.6		1.9		2.5		
t _h	Hold time	A or B after CLK↑	1		0.2		1		0.2		ns	
		CE̅ after CLK↑	1.2		0.2		1.2		0.2			

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH2952				SN74LVTH2952				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150		150		MHz	
t _{PLH}	CLKBA or CLKAB	A or B	1.2	4.8		5.5	1.3	2.9	4.6		5.3	ns
t _{PHL}			1.2	4.8		5.5	1.3	3.1	4.6		5.3	
t _{PZH}	OEBA or OEAB	A or B	1	4.8		5.9	1.1	2.6	4.6		5.8	ns
t _{PZL}			1	4.8		5.9	1.1	3	4.6		5.8	
t _{PHZ}	OEBA or OEAB	A or B	1.2	5.6		6	1.3	3.6	5.4		5.9	ns
t _{PLZ}			1.5	5.4		5.6	1.6	3.6	5.1		5.3	

\dagger All typical values are at $T_A = 25^\circ\text{C}$.

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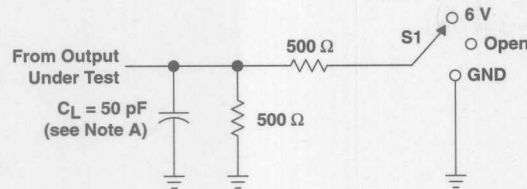


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SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

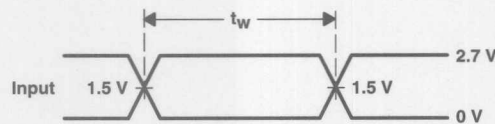
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PARAMETER MEASUREMENT INFORMATION

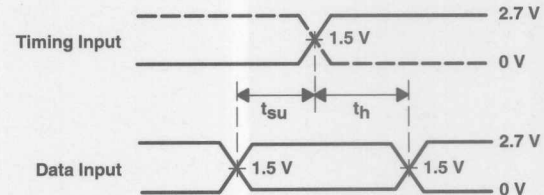


LOAD CIRCUIT FOR OUTPUTS

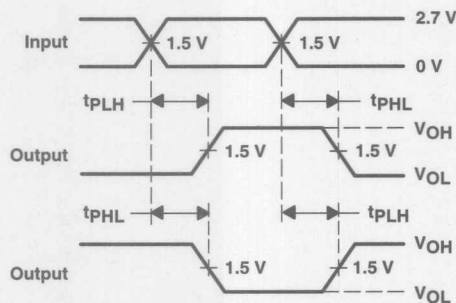
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



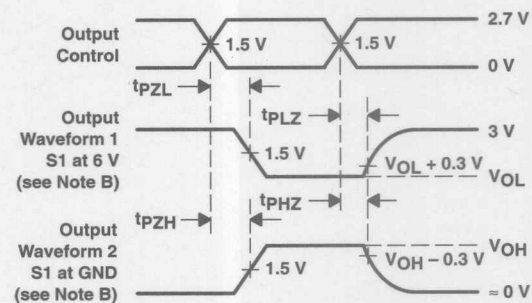
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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† The SN74LVTH16500, SN54LVTH16501, SN74LVTH16501, and SN74LVTH16835 are shown as product preview in this data book. The corresponding production data LVT data sheets for these devices are available through the TI home page at <http://www.ti.com/>.

SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16240 ... WD PACKAGE
SN74LVTH16240 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH16240 devices are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

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SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

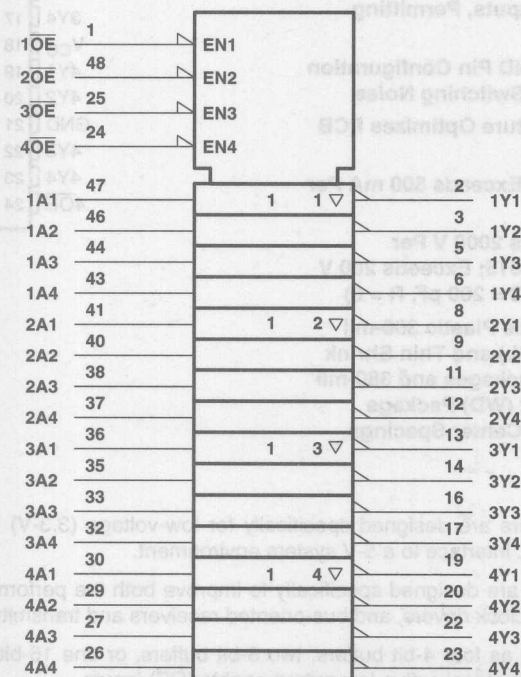
The SN54LVTH16240 is characterized for operation over the full military temperature range of -55°C to 125°C .

The SN74LVTH16240 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†

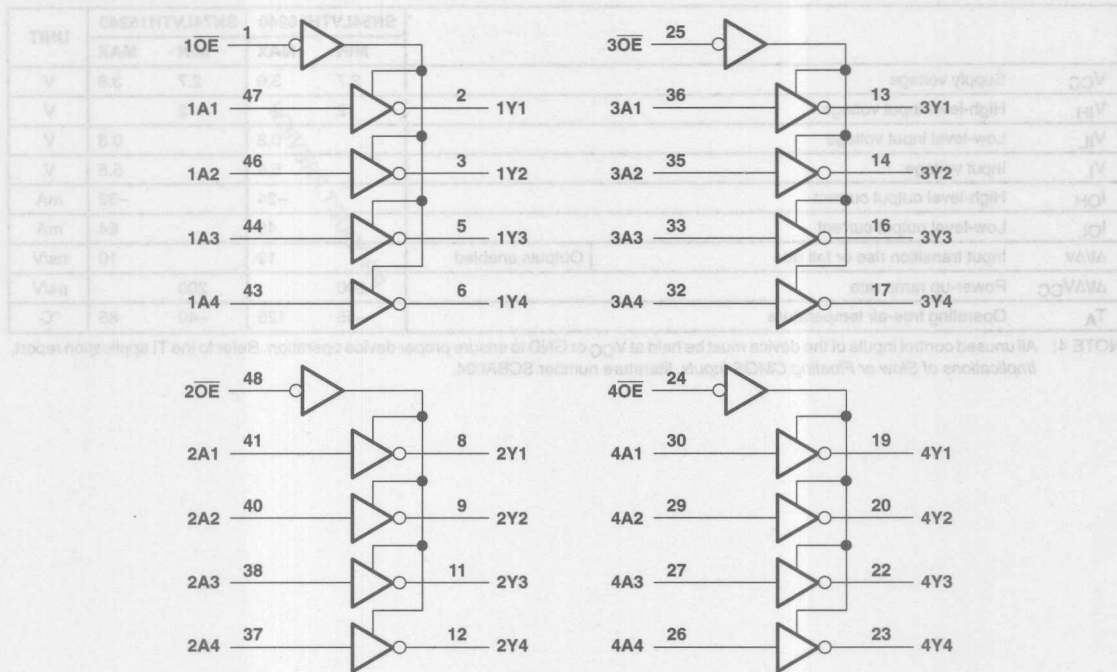


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16240	96 mA
SN74LVTH16240	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16240	48 mA
SN74LVTH16240	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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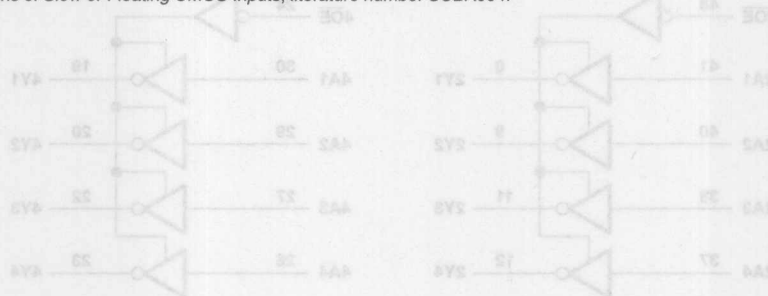
SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS684B – MARCH 1997 – REVISED MARCH 1998

recommended operating conditions (see Note 4)

		SN54LVTH16240		SN74LVTH16240		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		–24		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} –0.5 V to 4.5 V

Input voltage range, V_I (see Note 1) –0.5 V to 7 V

Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) –0.5 V to V_{CC} + 0.5 V

Voltage range applied to any output in the high state, V_O (see Note 1) –0.5 V to V_{CC} + 0.5 V

Current into any output in the low state, I_O (see Note 2) 88 mA

Current into any output in the high state, I_O (see Note 2) 158 mA

Input clamp current, I_{IK} (V_I > 0) 48 mA

Output clamp current, I_{OK} (V_O < 0) 48 mA

Package thermal impedance, θ_{JA} (see Note 3): DGG package 88°C/W

Package thermal impedance, θ_{JA} (see Note 3): D package 84°C/W

Storage temperature range, T_{stg} –65°C to 150°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ranges may be exceeded if the input and output clamp current ratings are observed.

2. This current flows only when the output is in the high state and V_O > V_{CC}.

3. The package thermal impedance is calculated in accordance with JEDEC 28.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16240			SN74LVTH16240			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
	$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4			0.4	
		$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$		0.55				
		$I_{OL} = 64\text{ mA}$					0.55	
I_I	Control inputs	$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	μA
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$		1			1	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		-5			-5	
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			μA
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_I	$V_I = 3\text{ V or } 0$			4			4	pF
C_O	$V_O = 3\text{ V or } 0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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3.6
3.6
4.2
4.6
4.7
4.4

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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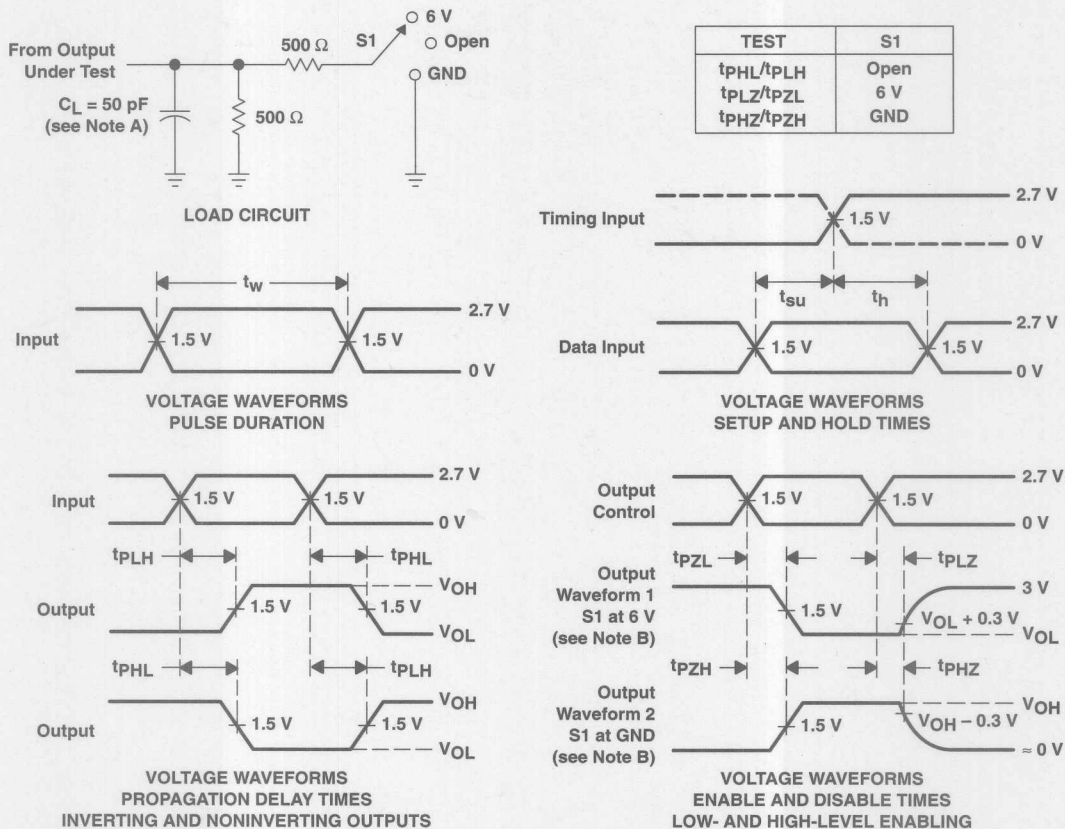
**TEXAS
INSTRUMENTS**

3-8

SN54LVTH16240, SN74LVTH16240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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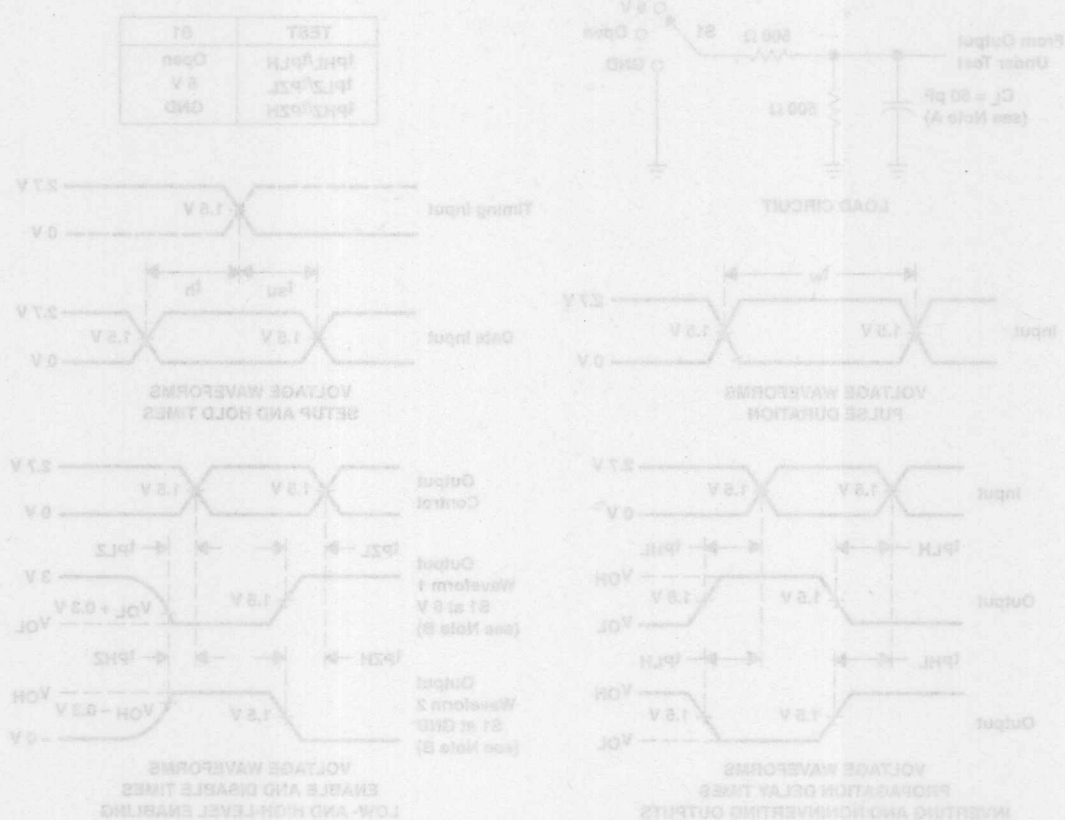
PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: PHL < 10 nsec, $\Delta V = 50\text{ mV}$, $t_r < 2.5\text{ ns}$, $t_f < 2.5\text{ ns}$.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162240 ... WD PACKAGE
SN74LVTH162240 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

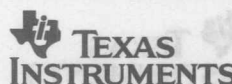
description

The 'LVTH162240 devices are 16-bit buffers/drivers designed specifically for low-voltage (3.3-V) V_{CC} operation and to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They have the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer and provide inverting outputs and symmetrical active-low output-enable (OE) inputs.

Widebus is a trademark of Texas Instruments Incorporated.

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SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH162240 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH162240 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

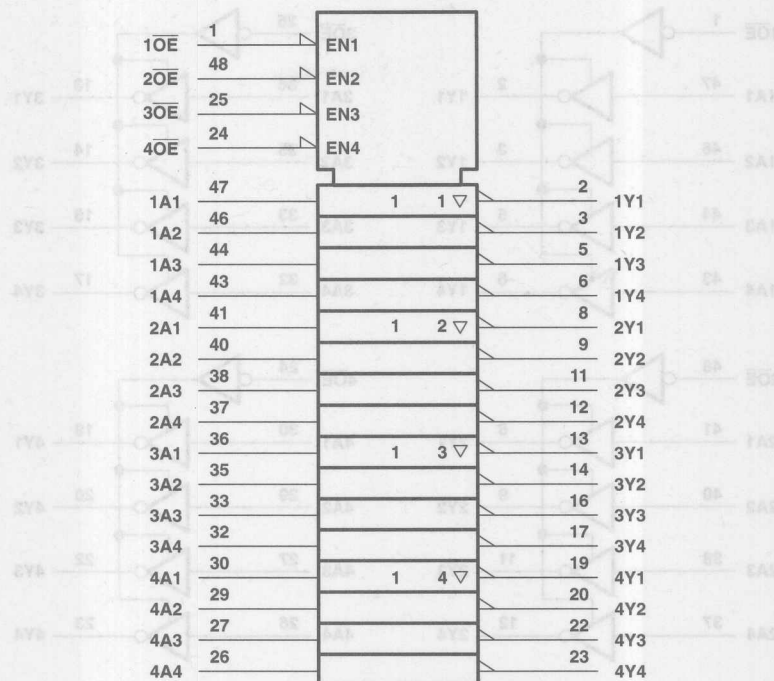
The LVTH162240 devices are 16-bit buffers/drivers designed specifically for low-voltage (3.3-V) V_{CC} operation and to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They have the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer and provide invert-
ing outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic symbol†



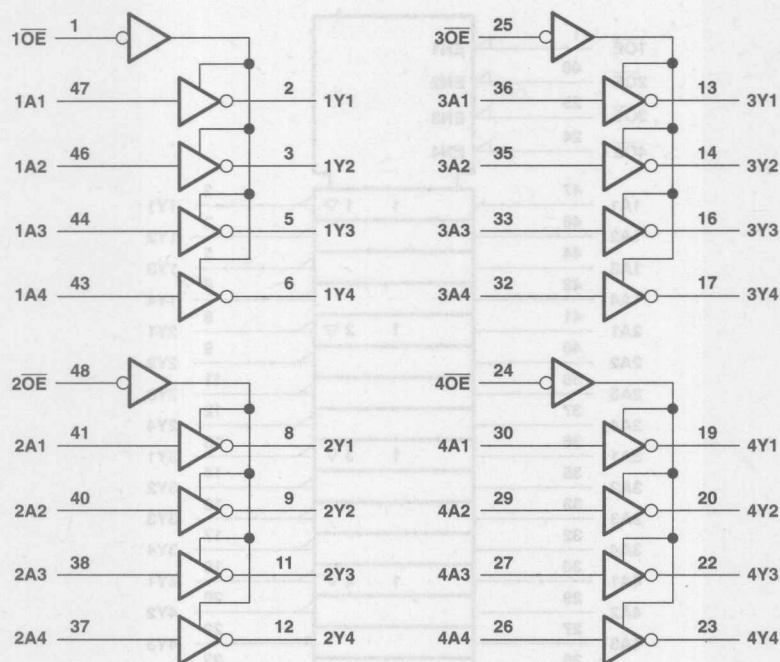
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Storage temperature range, T_{STG} -65°C to 150°C
 Package thermal impedance, θ_{JA} (see Note 3): DGG package 88°C/W
 DL package 64°C/W
 Input clamp current, I_{IK} ($V_I > 0$) -50 mA
 Output clamp current, I_{OK} ($V_O > 0$) -50 mA
 Current into any output in the high state, I_O (see Note 2) 30 mA
 Current into any output in the low state, I_{OL} 30 mA
 Voltage range applied to any output in the high state, V_O (see Note 1) -0.5 V to $V_{CC} + 0.5$ V
 or power-off state, V_O (see Note 1) -0.5 V to 7 V
 Voltage range applied to any output in the high-impedance state, V_Z (see Note 1) -0.5 V to 7 V
 Input voltage range, V_I (see Note 1) -0.5 V to 4.5 V
 Supply voltage range, V_{CC} 3.3 V to 4.5 V

NOTES: 1. The input and output negative-voltage ranges may be exceeded if the input and output clamp current ratings are observed.
 2. The current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JEDEC 81.

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	−0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LVTH162240		SN74LVTH162240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-12		-12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162240			SN74LVTH162240			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.7$ V,	$I_I = -18$ mA			-1.2			-1.2	V
V_{OH}		$V_{CC} = 3$ V,	$I_{OH} = -12$ mA	2			2			V
V_{OL}		$V_{CC} = 3$ V,	$I_{OL} = 12$ mA			0.8			0.8	V
I_I		$V_{CC} = 0$ or 3.6 V,	$V_I = 5.5$ V			10			10	μ A
	Control inputs	$V_{CC} = 3.6$ V,	$V_I = V_{CC}$ or GND			± 1			± 1	
	Data inputs	$V_{CC} = 3.6$ V	$V_I = V_{CC}$ $V_I = 0$			1 -5			1 -5	
I_{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V						± 100	μ A
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3$ V	$V_I = 0.8$ V	75			75			μ A
			$V_I = 2$ V	-75			-75			
I_{OZH}		$V_{CC} = 3.6$ V,	$V_O = 3$ V			5			5	μ A
I_{OZL}		$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			-5			-5	μ A
I_{OZPU}		$V_{CC} = 0$ to 1.5 V, $V_O = 0.5$ V to 3 V, $\overline{OE} = \text{don't care}$				$\pm 100^*$			± 100	μ A
I_{OZPD}		$V_{CC} = 1.5$ V to 0, $V_O = 0.5$ V to 3 V, $\overline{OE} = \text{don't care}$				$\pm 100^*$			± 100	μ A
I_{CC}		$V_{CC} = 3.6$ V, $I_O = 0$, $V_I = V_{CC}$ or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}^{\ddagger}		$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		$V_I = 3$ V or 0		4			4			pF
C_o		$V_O = 3$ V or 0		9			9			pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^{\circ}$ C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162240				SN74LVTH162240				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1	4.2		5	1	2.5	4		4.6	ns
t _{PHL}			1	4.2		5	1	2.9	4		4.6	
t _{PZH}	OE	Y	1	5		5.5	1	2.8	4.8		5.7	ns
t _{PZL}			1	4.9		5.1	1	2.8	4.7		4.9	
t _{PHZ}	OE	Y	1.9	4.9		5.4	2	3.5	4.7		5.2	ns
t _{PLZ}			1.9	4.7		4.8	2	3.4	4.5		4.5	
t _{sk(o)} ‡									0.5		0.5	ns

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

UNIT	SN54LVTH162240				SN74LVTH162240				TEST CONDITIONS		PARAMETER
	MAX	TYP	MIN	MAX	MAX	TYP	MIN	MAX			
V	1.2			1.2					$V_{CC} = 3.3 \text{ V}$ $I_L = -18 \text{ mA}$		V_{IK}
V									$V_{CC} = 3 \text{ V}$ $I_{OL} = -15 \text{ mA}$		V_{OH}
V	0.5			0.5					$V_{CC} = 3 \text{ V}$ $I_{OL} = 15 \text{ mA}$		V_{OL}
A	10			10					$V_{CC} = 0 \text{ or } 3.3 \text{ V}$ $V_I = 3.3 \text{ V}$		Control inputs
	1			1					$V_I = V_{CC} \text{ or GND}$ $V_O = V_{CC} \text{ or GND}$		
	1			1					$V_I = V_{CC}$ $V_O = 3.3 \text{ V}$		
	1			1					$V_I = 0$ $V_O = 3.3 \text{ V}$		
A	±100			±100					$V_{CC} = 0$ $V_I = V_O = 0 \text{ or } 3.3 \text{ V}$		I_{OZ}
A									$V_{CC} = 3 \text{ V}$ $V_I = 3.3 \text{ V}$		Data inputs
									$V_I = 0$ $V_O = 3.3 \text{ V}$		
A	3			3					$V_{CC} = 3.3 \text{ V}$ $V_O = 3.3 \text{ V}$		I_{OSH}
A	3			3					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		I_{OSL}
A	±150			±150					$V_{CC} = 0 \text{ or } 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		I_{OZP}
A	±100			±100					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		I_{OZM}
A	0.15			0.15					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		t_{CO}
	3			3					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		
	0.15			0.15					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		
A	0.5			0.5					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		t_{COF}
C	3			3					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		C_{in}
C	3			3					$V_{CC} = 3.3 \text{ V}$ $V_O = 0 \text{ or } 3.3 \text{ V}$		C_{out}

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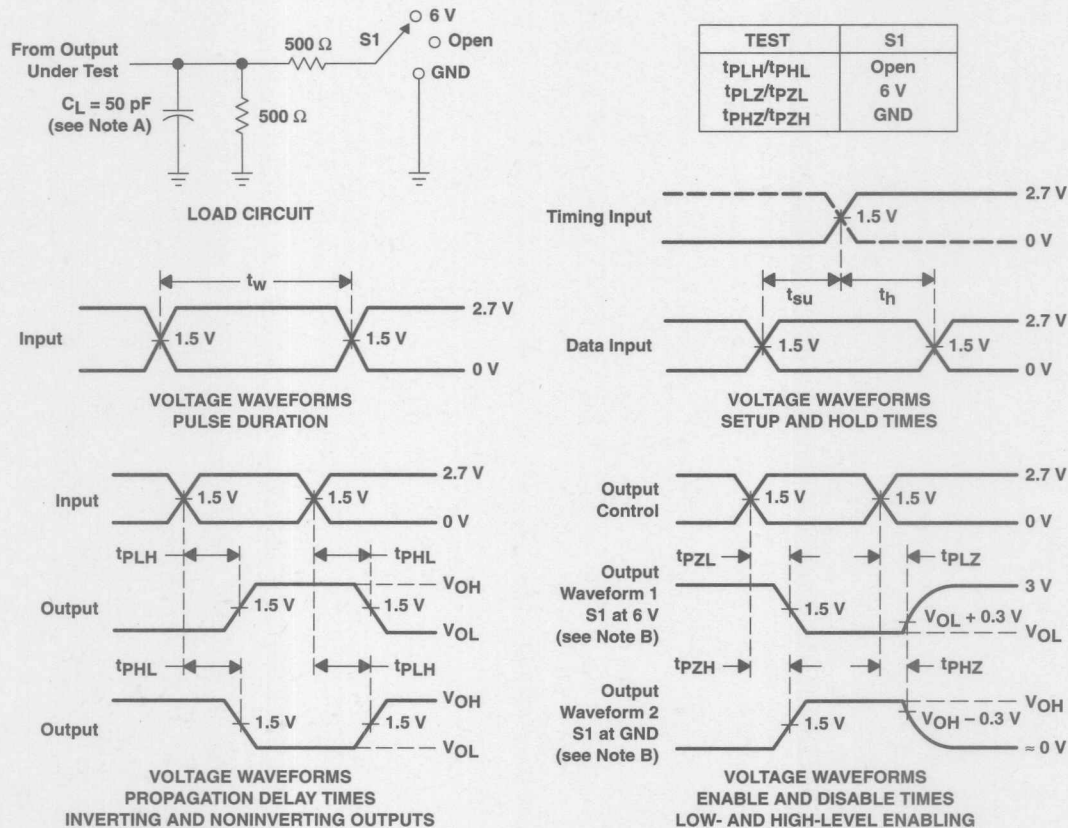


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SN54LVTH162240, SN74LVTH162240
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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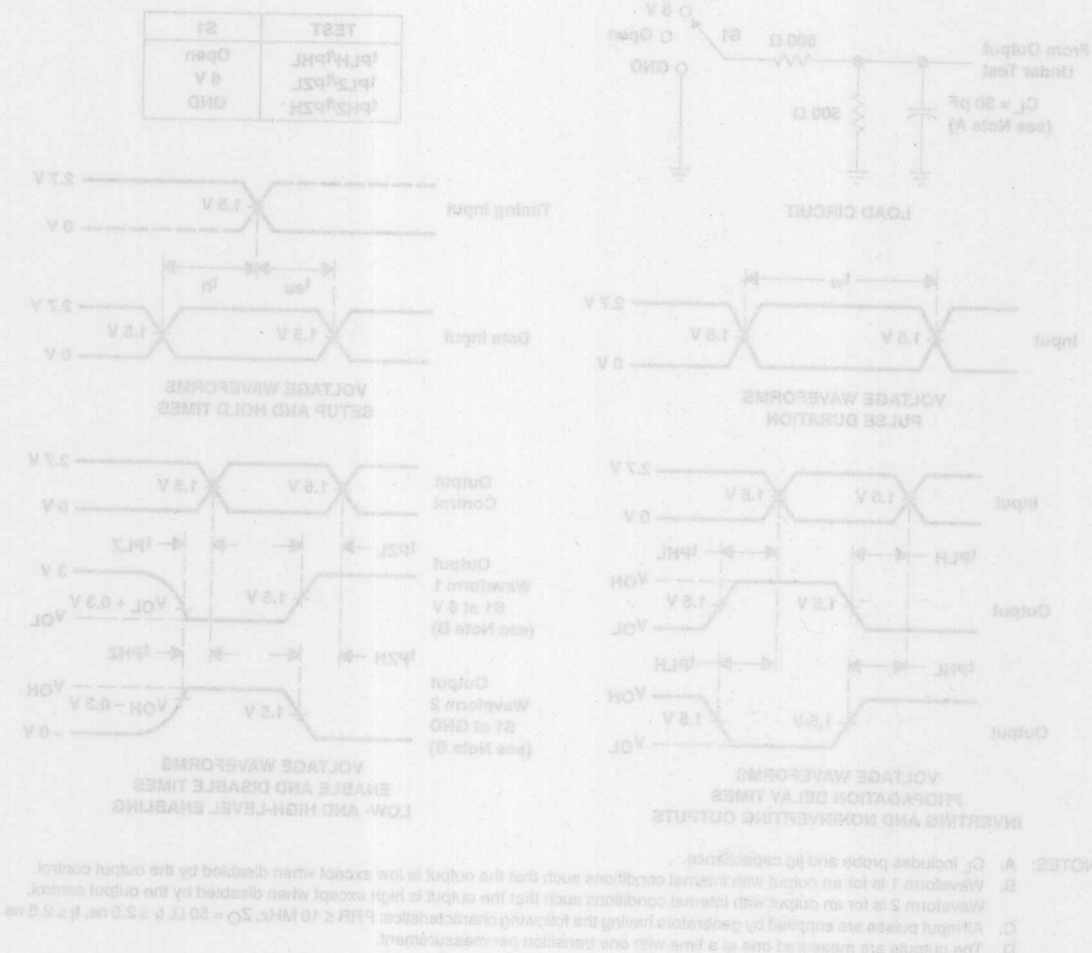
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16241 ... WD PACKAGE
SN74LVTH16241 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

description

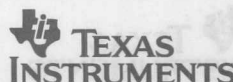
These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide noninverting outputs and complementary output-enable (OE and \overline{OE}) inputs.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

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SN54LVTH16241, SN74LVTH16241
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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16241 is characterized for operation over the full military temperature range of -55°C to 125°C .

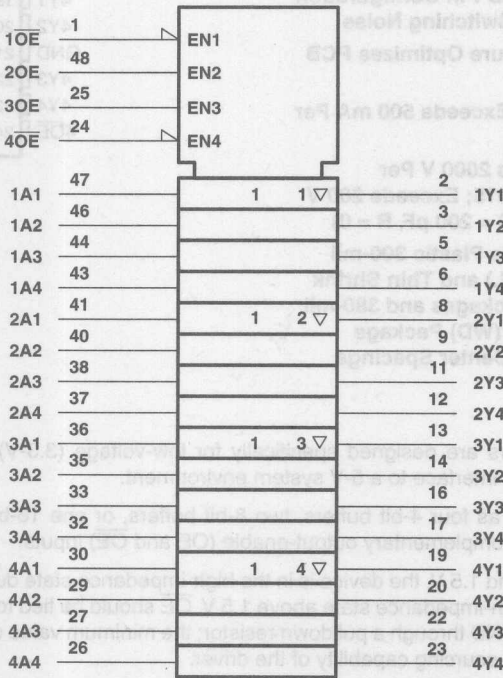
The SN74LVTH16241 is characterized for operation from -40°C to 85°C .

FUNCTION TABLES

INPUTS		OUTPUTS	
1OE, 4OE	1A, 4A	1Y, 4Y	
L	H	H	
L	L	L	
H	X	Z	

INPUTS		OUTPUTS	
2OE, 3OE	2A, 3A	2Y, 3Y	
H	H	H	
H	L	L	
L	X	Z	

logic symbol†

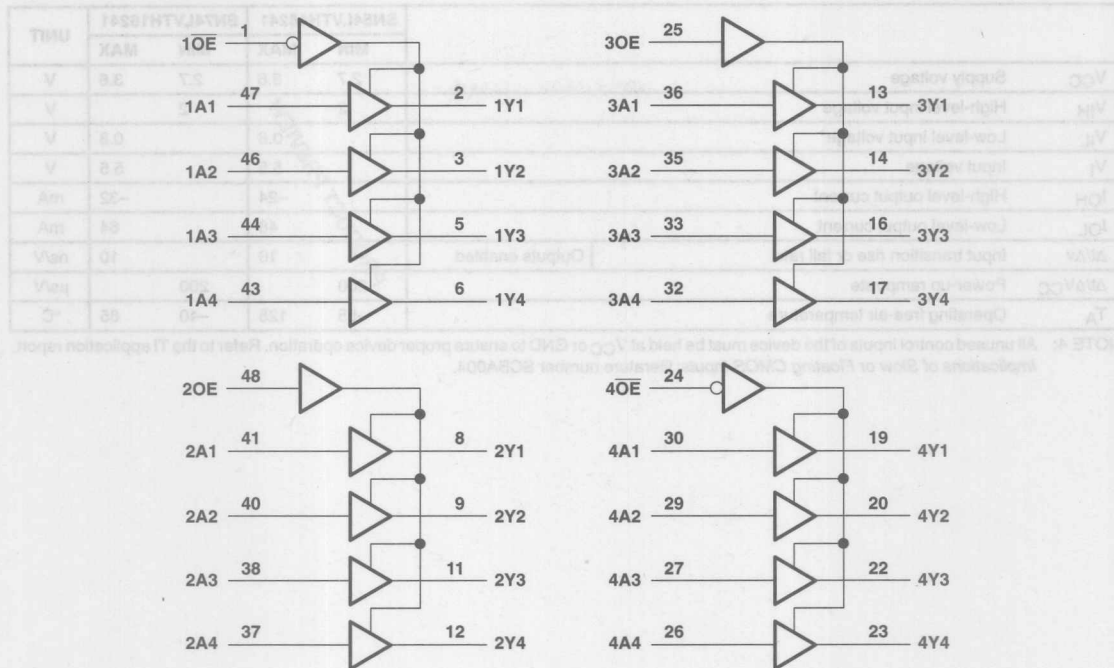


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16241	96 mA
SN74LVTH16241	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16241	48 mA
SN74LVTH16241	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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recommended operating conditions (see Note 4)

		SN54LVTH16241		SN74LVTH16241		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		–24		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate			200	200	μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH16241, SN74LVTH16241
3.3-V ABT 16-BIT BUFFERS/DRIVERS
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

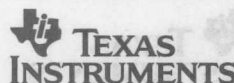
PARAMETER	TEST CONDITIONS	SN54LVTH16241			SN74LVTH16241			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2						
	$I_{OH} = -32 \text{ mA}$				2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$		0.5			0.5	
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$		0.4			0.4	
		$I_{OL} = 32 \text{ mA}$		0.5			0.5	
		$I_{OL} = 48 \text{ mA}$		0.55				
		$I_{OL} = 64 \text{ mA}$					0.55	
I_I		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		10			10	μA
	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$ $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$			± 100			± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75		75			μA
		$V_I = 2 \text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $OE/O\bar{E} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $OE/O\bar{E} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$		4			4		pF
C_o	$V_O = 3 \text{ V or } 0$		9			9		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16241				SN74LVTH16241				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1.1	3.7		4	1.2	2.6	3.5		3.8	ns
t _{PHL}			1.1	3.7		4	1.2	2.2	3.5		3.8	
t _{PZH}	OE or OE	Y	1.1	4.7		5.3	1.2	3.2	4.5		5.1	ns
t _{PZL}			1.1	4.7		5.2	1.2	3.2	4.5		4.9	
t _{PHZ}	OE or OE	Y	1.9	5.5		6.1	2	3.7	5.3		5.9	ns
t _{PLZ}			1.9	5.2		5.7	2	3.4	4.9		5.4	
t _{sk(o)} ‡									0.5		0.5	ns

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

A ₁	10	10	V _{CC} = 0 or 3.3 V		V _{CC} = 0 or 3.3 V		Control inputs	Data inputs	V _{CC} = 3.3 V	V _I = V _{CC}	V _I = 0	V _I = 0 or 3.3 V	V _{CC} = 0	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V	V _{CC} = 3.3 V
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* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.
‡ This is the increase in supply current for each input that is the specified TTL voltage level, not the V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

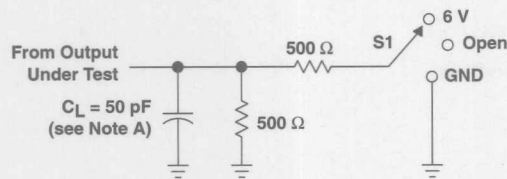


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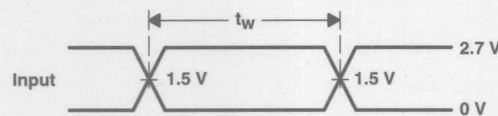
SN54LVTH16241, SN74LVTH16241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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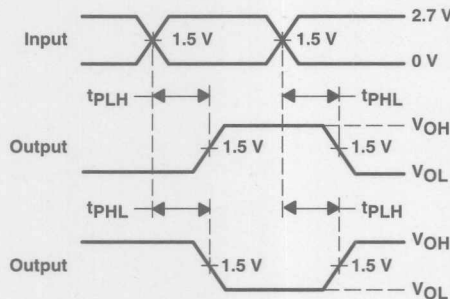
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

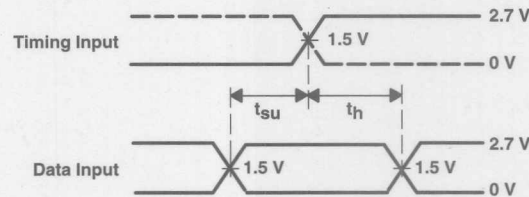


VOLTAGE WAVEFORMS
PULSE DURATION

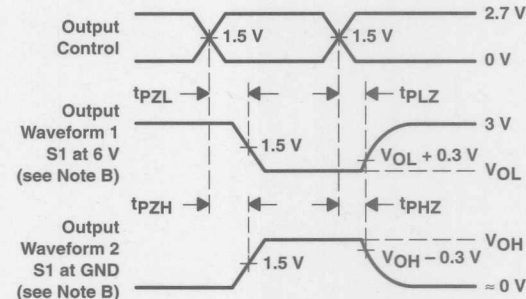


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

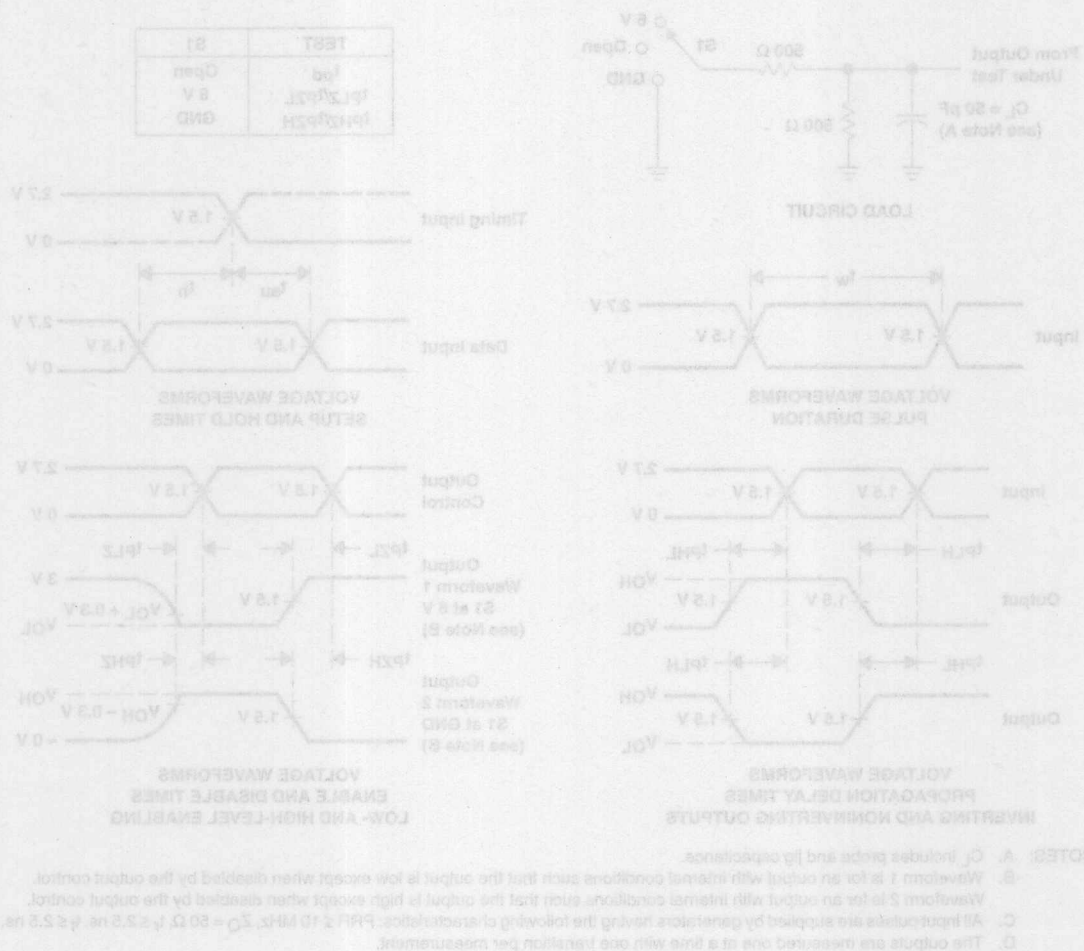


Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- Output Ports Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162241 ... WD PACKAGE
SN74LVTH162241 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

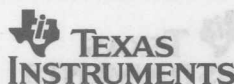
description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide noninverting outputs and complementary output-enable (OE and \overline{OE}) inputs.

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SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH162241 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH162241 is characterized for operation from -40°C to 85°C.

FUNCTION TABLES

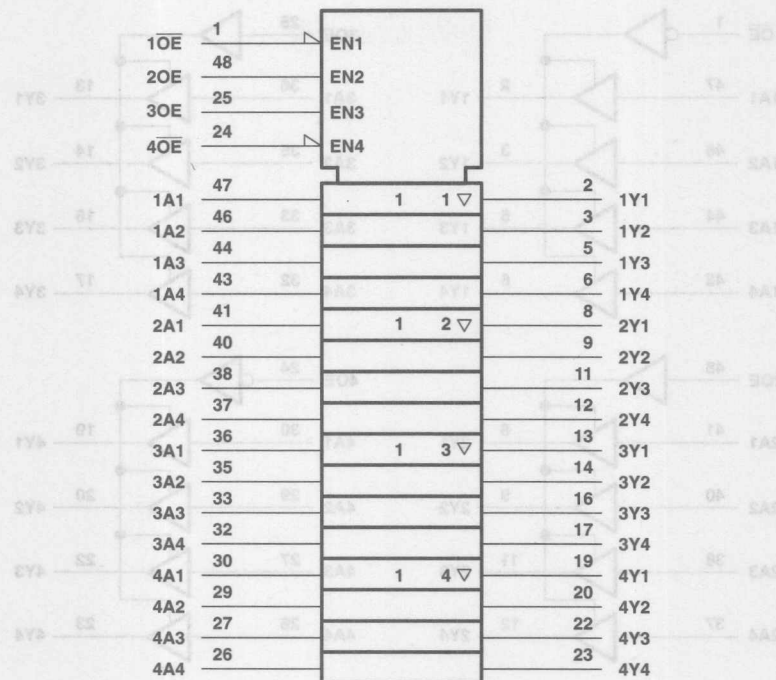
INPUTS		OUTPUTS
1OE, 4OE	1A, 4A	1Y, 4Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUTS
2OE, 3OE	2A, 3A	2Y, 3Y
H	H	H
H	L	L
L	X	Z

The 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The device provides noninverting outputs and complementary output-enable (OE and \overline{OE}) inputs.

SN54LVTH162241, SN74LVTH162241
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS
 SCBS692C – MAY 1997 – REVISED MAY 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating temperature range (unless otherwise specified)

Supply voltage range, V_{CC} -0.5 V to 4.5 V

Input voltage range, V_I (see Note 1) -0.5 V to V_{CC}

Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) -0.5 V to V_{CC}

Voltage range applied to any output in the high state, V_O (see Note 1) -0.5 V to $V_{CC} + 0.5$ V

Current into any output in the low state, I_O 30 mA

Current into any output in the high state, I_O (see Note 2) 30 mA

Input clamp current, I_{IK} ($V_I < 0$) -50 mA

Output clamp current, I_{OK} ($V_O < 0$) -50 mA

Package thermal impedance, θ_{JA} (see Note 3): DGG package 89°C/W

DI package 84°C/W

Storage temperature range, T_{STG} -55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and should not be exceeded for extended periods. Recommended operating conditions, "recommended operating conditions," is not limited. Exposure to absolute maximum ratings may be necessary for test purposes. Conditions for extended periods may affect device reliability.

NOTES:

1. The input and output voltage range may be extended to the input and output clamp current range if observed.
2. The current flow only when the output is in the high state and $V_{CC} = V_{OH}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

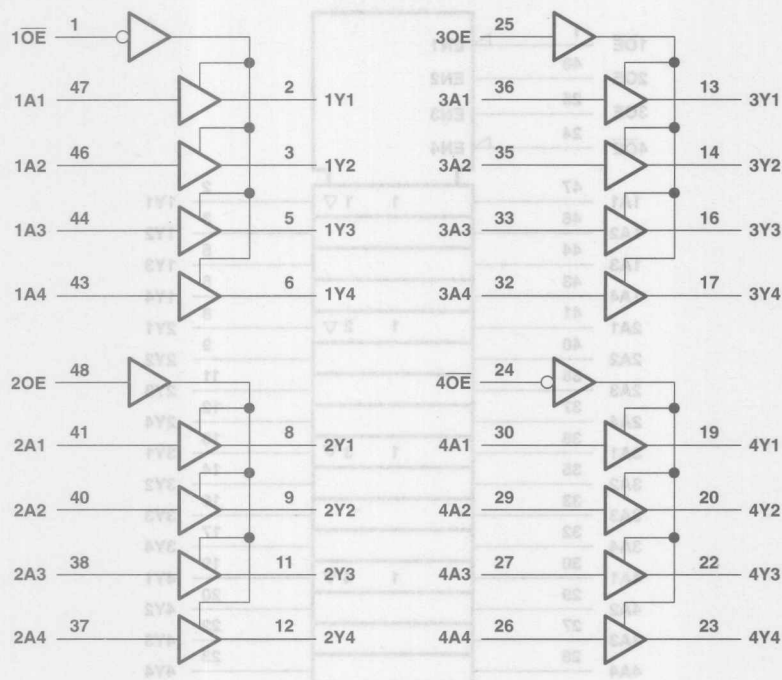


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SN54LVTH162241, SN74LVTH162241
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54LVTH162241		SN74LVTH162241		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-12		-12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)


PARAMETER		TEST CONDITIONS		SN54LVTH162241		SN74LVTH162241		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA	-1.2		-1.2		V
V _{OH}		V _{CC} = 3 V,	I _{OH} = -12 mA	2		2		V
V _{OL}		V _{CC} = 3 V,	I _{OL} = 12 mA	0.8		0.8		V
I _I		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	10		10		µA
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	±1		±1		
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}	1		1		
			V _I = 0	-5		-5		
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V	±100		±100		µA
I _{I(hold)}	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75		µA
			V _I = 2 V	-75		-75		
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V	5		5		µA
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V	-5		-5		µA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		µA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		µA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.19		0.19		mA
			Outputs low	5		5		
			Outputs disabled	0.19		0.19		
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA
C _I		V _I = 3 V or 0		4		4		pF
C _O		V _O = 3 V or 0		9		9		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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 **TEXAS
INSTRUMENTS**

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SN54LVTH162241, SN74LVTH162241 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS692C – MAY 1997 – REVISED MAY 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162241				SN74LVTH162241				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1.3	4.3		4.9	1.4	3	4.1		4.7	ns
t _{PHL}			1.3	4.3		4.9	1.4	2.4	4.1		4.7	
t _{PZH}	\overline{OE} or OE	Y	1.1	5.2		5.9	1.2	3.5	4.9		5.7	ns
t _{PZL}			1.4	5		5.4	1.5	3.5	4.8		5.2	
t _{PHZ}	\overline{OE} or OE	Y	1.9	5.5		6.2	2	3.7	5.3		5.9	ns
t _{PLZ}			1.9	5.2		5.7	2	3.6	4.9		5.4	
t _{sk(o)} ‡									0.5		0.5	ns

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

UNIT	SN54LVTH162241			SN74LVTH162241			TEST CONDITIONS	PARAMETER
	MIN	TYP†	MAX	MIN	TYP†	MAX		
V	-1.5		-1.5				$V_{CC} = 3.3$ V $I_L = -15$ mA	V_{IK}
V							$V_{CC} = 3.3$ V $I_{OH} = -15$ mA	V_{OH}
V	0.0		0.0				$V_{CC} = 3.3$ V $I_{OL} = 15$ mA	V_{OL}
A _{ii}	10		10				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Control inputs
	±1		±1				$V_{CC} = 3.3$ V $V_I = V_{CC}$ or GND	
	1		1				$V_{CC} = 3.3$ V $V_I = V_{CC}$	
	±5		±5				$V_{CC} = 3.3$ V $V_I = 0$	
A _{ii}	0.01±		0.01±				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	15		15				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	
A _{ii}	±15		±15				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	5		5				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	
A _{ii}	±5		±5				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	0.01±		0.01±				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	
A _{ii}	0.01±		0.01±				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	0.19		0.19				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	
A _{ii}	5		5				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	0.19		0.19				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	
A _{ii}	0.5		0.5				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	4		4				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	
A _{ii}	5		5				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	Data inputs
A _{ii}	5		5				$V_{CC} = 3.3$ V $V_I = 0$ or 3.3 V	

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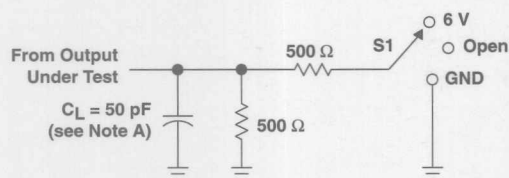


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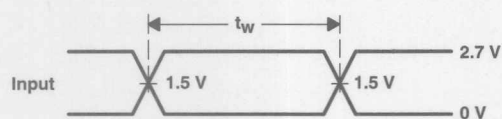
SN54LVTH162241, SN74LVTH162241
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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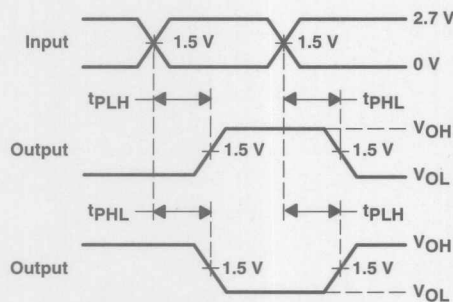
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

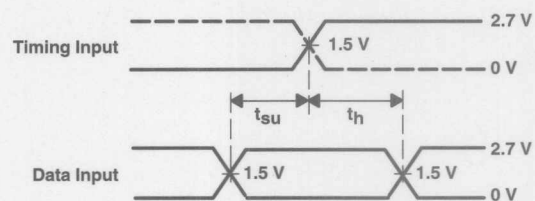


VOLTAGE WAVEFORMS
PULSE DURATION

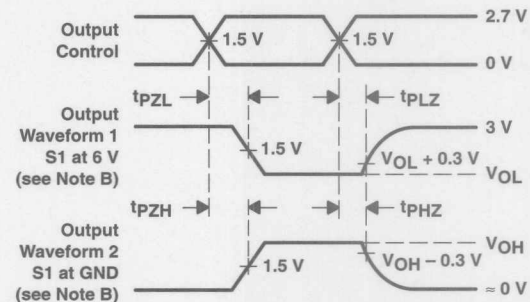


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

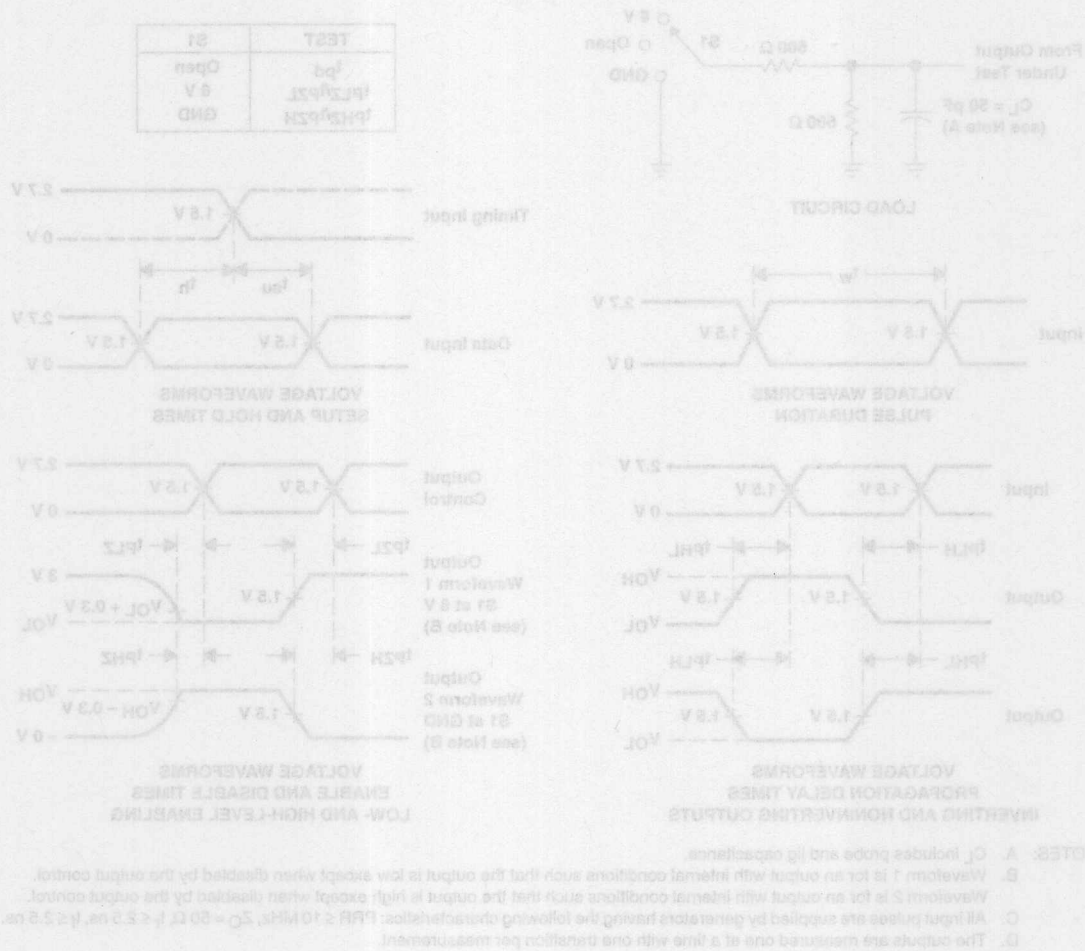


Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142K – MAY 1992 – REVISED MARCH 1998

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16244A ... WD PACKAGE
SN74LVTH16244A ... DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

description

The 'LVTH16244A devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5-V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5-V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16244A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16244A is characterized for operation from -40°C to 85°C .

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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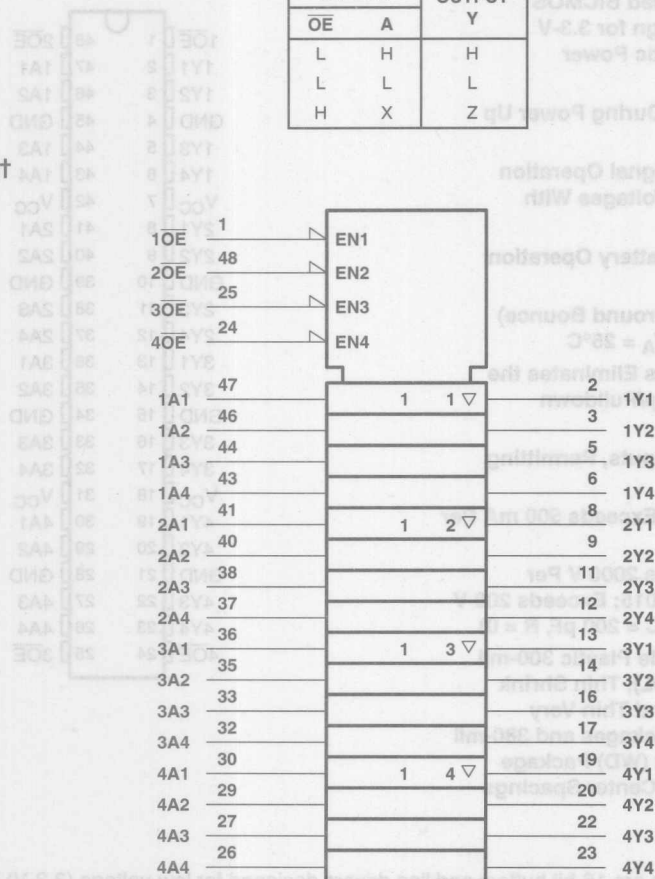
SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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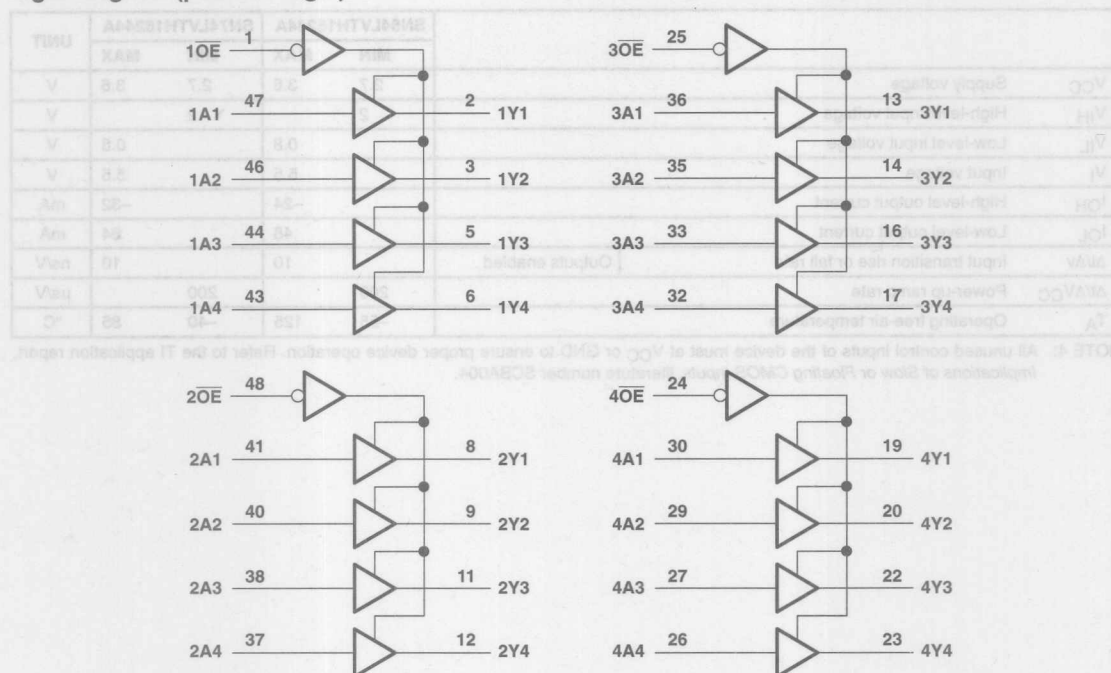
SN54LVTH16244A, SN74LVTH16244A

3.3-V ABT 16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

SCBS142K - MAY 1992 - REVISED MARCH 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16244A	96 mA
SN74LVTH16244A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16244A	48 mA
SN74LVTH16244A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.



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SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

			SN54LVTH16244A		SN74LVTH16244A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage			5.5		5.5	V
I _{OH}	High-level output current			–24		–32	mA
I _{OL}	Low-level output current			48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	–0.5 V to 4.8 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V _O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V _O (see Note 1)	–0.5 V to V _{CC} + 0.8 V
Current into any output in the low state, I _O	SN54LVTH16244A: 98 mA SN74LVTH16244A: 128 mA
Current into any output in the high state, I _O (see Note 2)	SN54LVTH16244A: 48 mA SN74LVTH16244A: 84 mA
Input clamp current, I _{IK} (V _I < 0)	–80 mA
Output clamp current, I _{OK} (V _O > 0)	–80 mA
Package thermal impedance, θ _{JA} (see Note 3): DGG package	88°C/W
Package thermal impedance, θ _{JA} (see Note 3): DGV package	83°C/W
Package thermal impedance, θ _{JA} (see Note 3): DL package	84°C/W
Storage temperature range, T _{stg}	–85°C to 150°C

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

3. The current flows only when the output is in the high state and V_O = V_{CC}.

4. The package thermal impedance is calculated in accordance with JEDEC J-STD-71.

SN54LVTH16244A, SN74LVTH16244A
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

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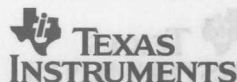
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16244A			SN74LVTH16244A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2						
					2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$			0.2			0.2	V
				0.5			0.5	
	$V_{CC} = 3 \text{ V}$			0.4			0.4	
				0.5			0.5	
				0.55			0.55	
I_I	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		50			10	μA
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$		1			1	
		$V_I = 0$		-5			-5	
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75		75			μA
		$V_I = 2 \text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND			0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$		4			4		pF
C_o	$V_O = 3 \text{ V or } 0$		9			9		pF

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142K – MAY 1992 – REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16244A				SN74LVTH16244A				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1.1	4.4		4.6	1.2	2.3	3.2		3.7	ns
t _{PHL}			1.1	3.6		3.9	1.2	2	3.2		3.7	
t _{PZH}	OE	Y	1.1	4.6		5.4	1.2	2.6	4		5	ns
t _{PZL}			1.1	5.4		6.2	1.2	2.7	4		5	
t _{PHZ}	OE	Y	1.6	5.7		6.2	2.2	3.3	4.5		5	ns
t _{PLZ}			1.2	5		4.7	2	3.1	4.2		4.4	
t _{sk(o)} ‡									0.5			ns

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

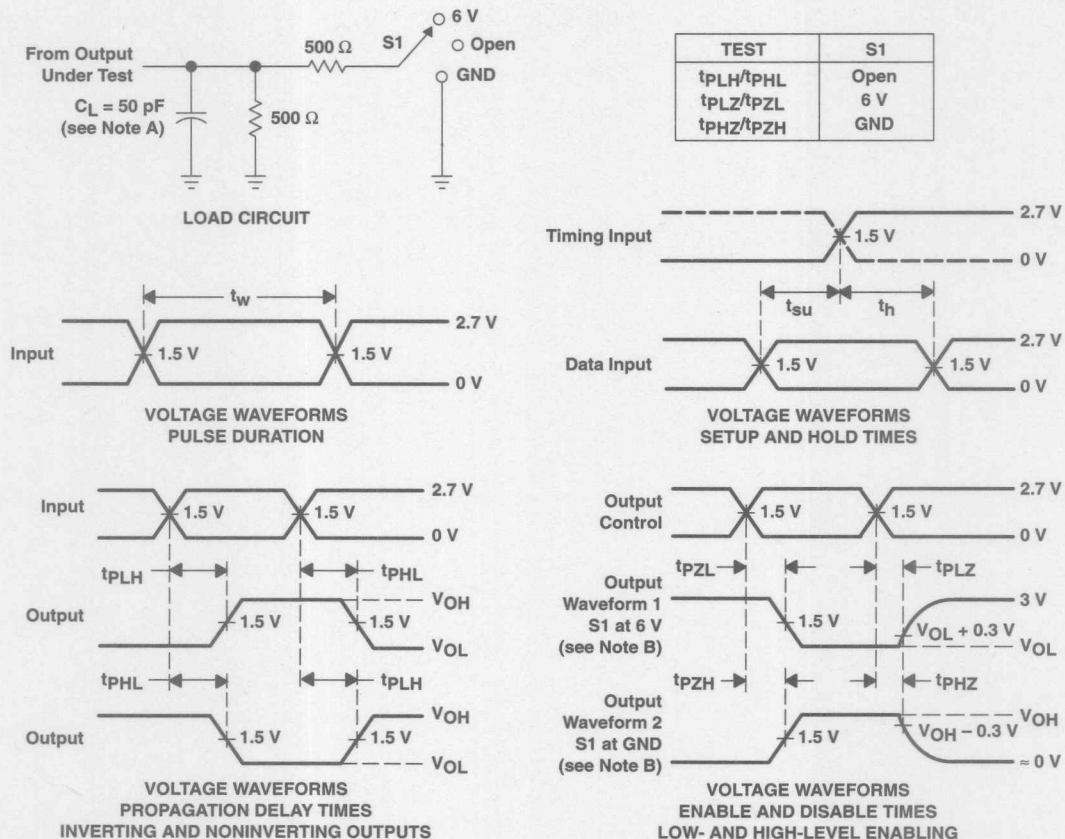
‡ Skew between any two outputs of the same package switching in the same direction

A ₁₄	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₁₃	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₁₂	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₁₁	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₁₀	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₉	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₈	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₇	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₆	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₅	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₄	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₃	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₂	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
A ₁	10	50	$V_{CC} = 0$ or 3.3 V		$V_{CC} = 0$ or 3.3 V		Data inputs
	11	11	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	1	1	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		
	2	2	$V_{CC} = 3.3$ V		$V_{CC} = 3.3$ V		

SN54LVTH16244A, SN74LVTH16244A 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS142K – MAY 1992 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS WITH 3-STATE OUTPUTS

SCBS2581 - JUNE 1993 - REVISED MARCH 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162244...WD PACKAGE
SN74LVTH162244...DGG OR DL PACKAGE
(TOP VIEW)

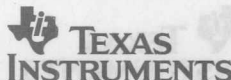
1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

description

The 'LVTH162244 devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

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PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54LVTH162244, SN74LVTH162244 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS WITH 3-STATE OUTPUTS

SCBS2581 – JUNE 1993 – REVISED MARCH 1998

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

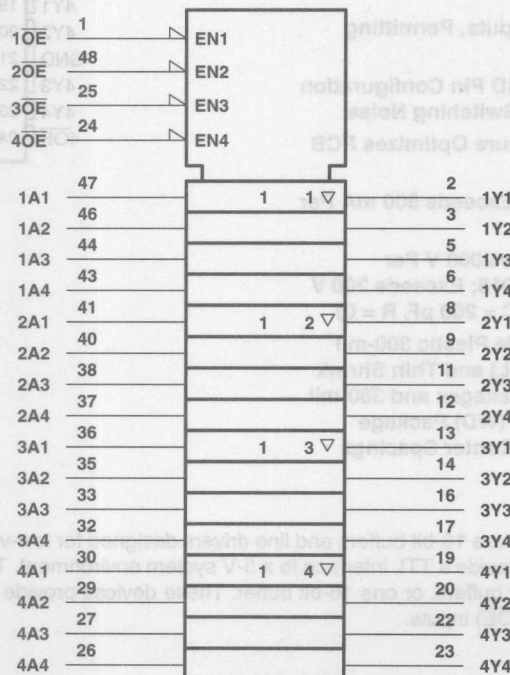
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LVTH162244 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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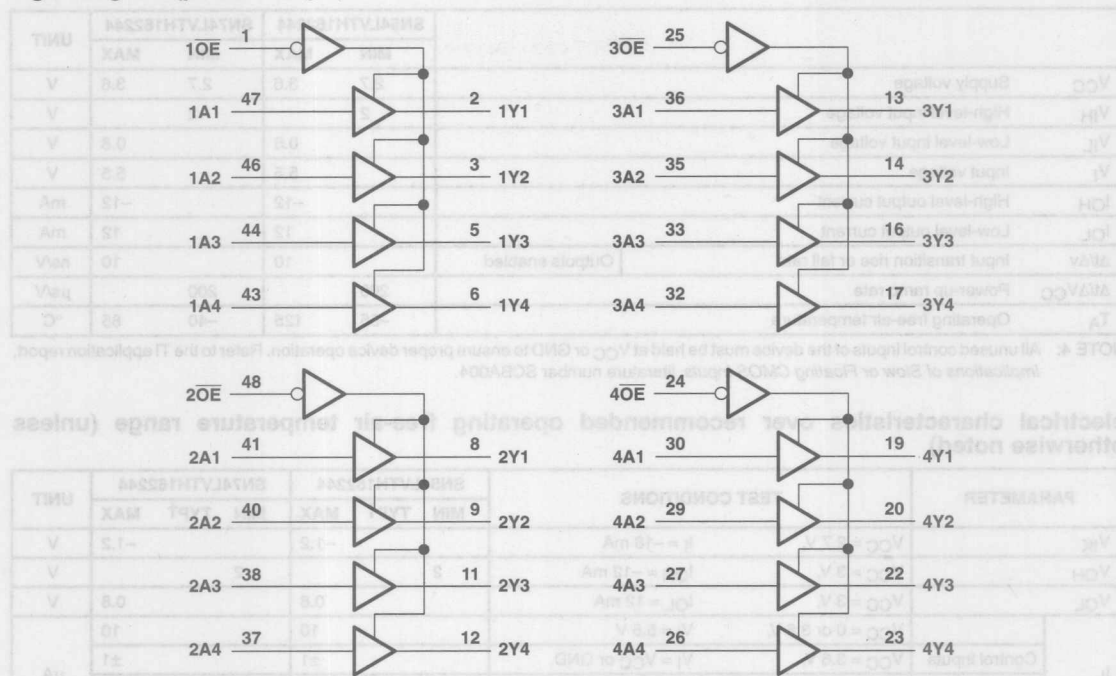


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SN54LVTH162244, SN74LVTH162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS WITH 3-STATE OUTPUTS

SCBS2581 - JUNE 1993 - REVISED MARCH 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.



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SN54LVTH162244, SN74LVTH162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS WITH 3-STATE OUTPUTS

SCBS2581 – JUNE 1993 – REVISED MARCH 1998

recommended operating conditions (see Note 4)

		SN54LVTH162244		SN74LVTH162244		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		–12		–12	mA
I _{OL}	Low-level output current		12		12	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162244			SN74LVTH162244			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 2.7 V, I _I = –18 mA				–1.2			–1.2	V
V _{OH}		V _{CC} = 3 V, I _{OH} = –12 mA		2			2			V
V _{OL}		V _{CC} = 3 V, I _{OL} = 12 mA				0.8			0.8	V
I _I		V _{CC} = 0 or 3.6 V, V _I = 5.5 V				10			10	μA
	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND				±1			±1	
	Data inputs	V _{CC} = 3.6 V, V _I = V _{CC} V _I = 0				1 –5			1 –5	
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V							±100	μA
I _I (hold)	A inputs	V _{CC} = 3 V, V _I = 0.8 V		75			75			μA
		V _{CC} = 3 V, V _I = 2 V		–75			–75			
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V				5			5	μA
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V				–5			–5	μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care				±100*			±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care				±100*			±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND				0.2			0.2	mA
C _I		V _I = 3 V or 0				4			4	pF
C _O		V _O = 3 V or 0				9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH162244, SN74LVTH162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTSWITH 3-STATE OUTPUTS

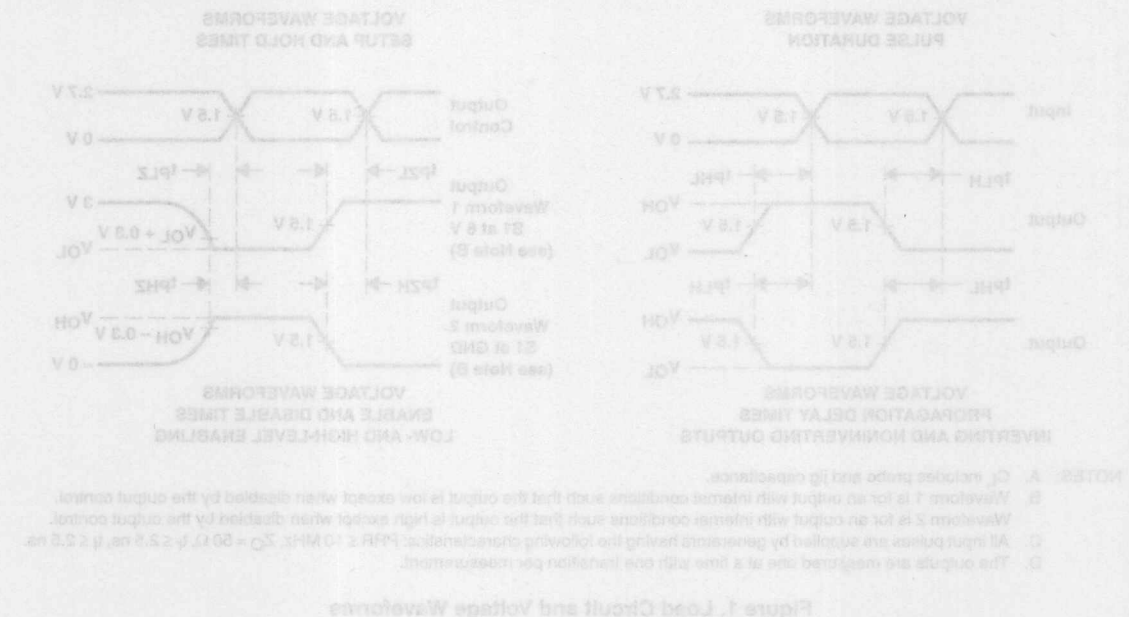
SCBS258I - JUNE 1993 - REVISED MARCH 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162244				SN74LVTH162244				UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
tPLH	A	Y	1.1	4.6		5.1	1.4	3.4	4	4.8	ns
tPHL			1.1	3.9		4.5	1.2	2.9	3.6	4.1	
tPZH	OE	Y	1.1	5.4		6.7	1.2	3.9	5.1	6.5	ns
tPZL			1.3	4.9		6.1	1.4	3.8	4.5	5.8	
tPHZ	OE	Y	1.6	5.5		5.8	2.2	4.4	5	5.4	ns
tPLZ			1.2	5.9		5.8	2	4.2	5	5.4	
t _{sk(o)} ‡									0.5		ns

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

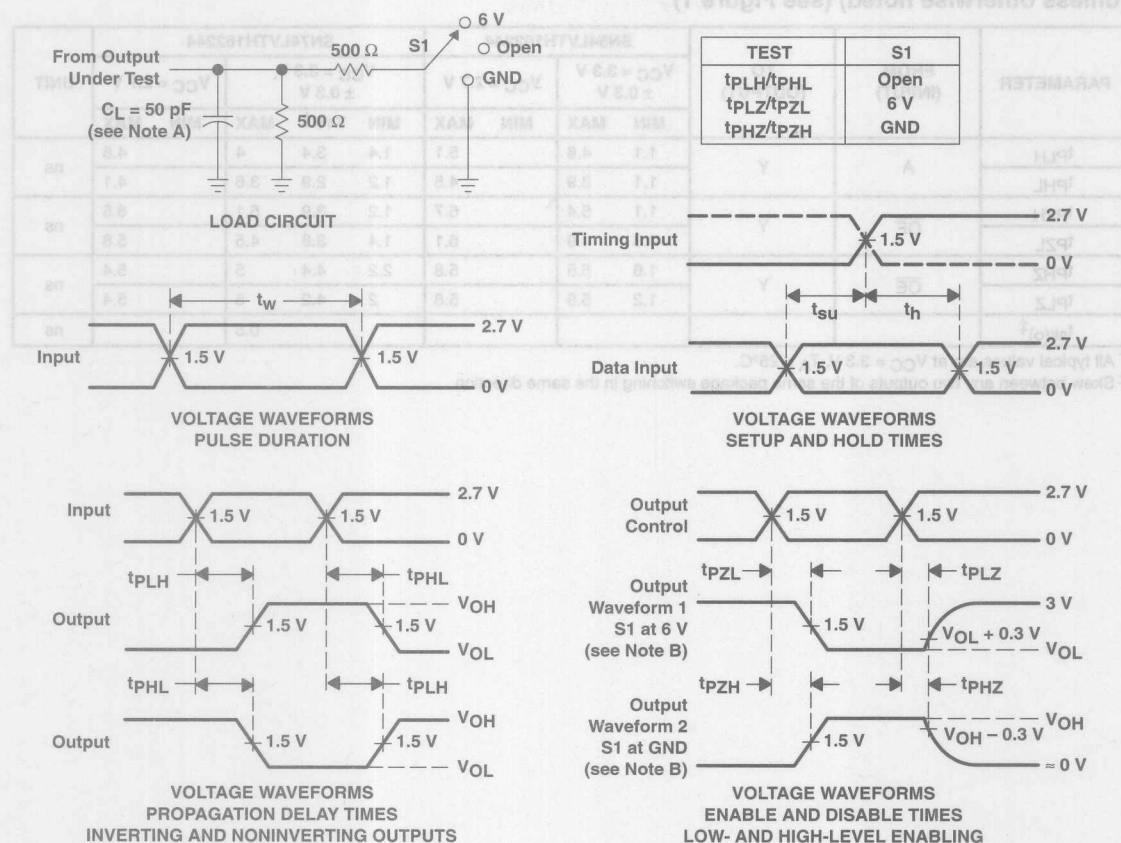
‡ Skew between any two outputs of the same package switching in the same direction



SN54LVTH162244, SN74LVTH162244
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTSWITH 3-STATE OUTPUTS

SCBS2581 – JUNE 1993 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16245A, SN74LVTH16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143K – MAY 1992 – REVISED APRIL 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16245A . . . WD PACKAGE
SN74LVTH16245A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1OE
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2OE

description

The 'LVTH16245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the devices so that the buses are effectively isolated.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
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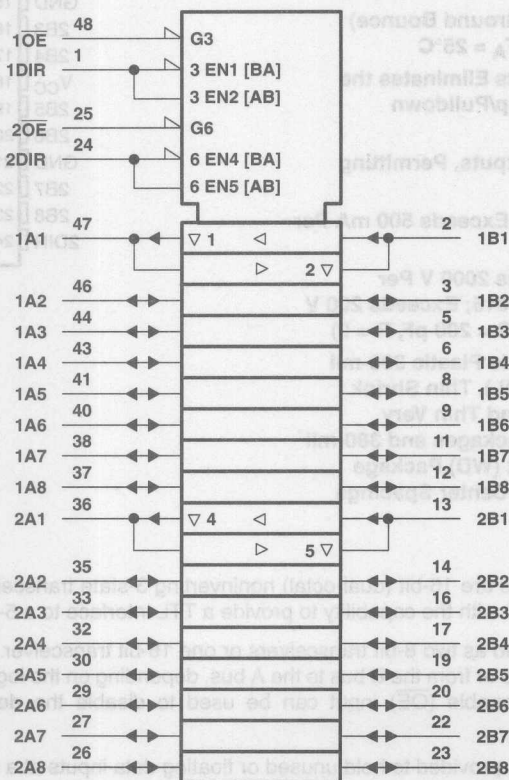
When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16245A is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†

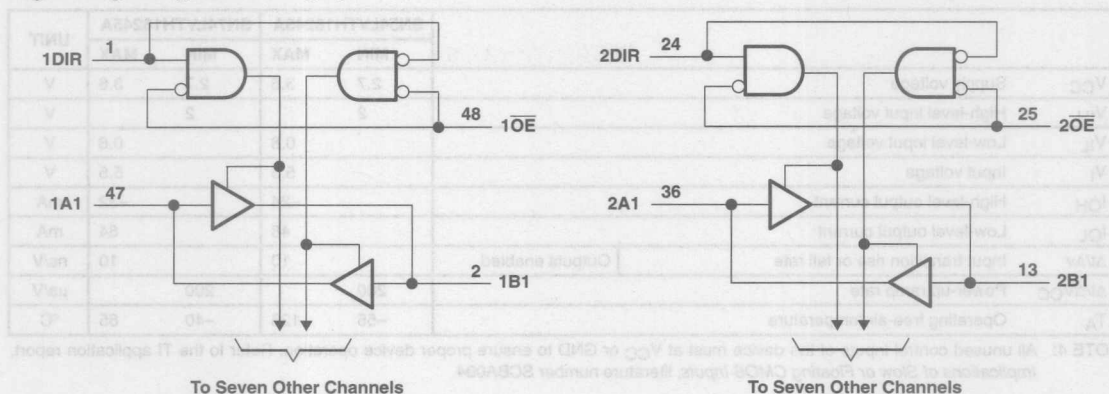


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTH16245A, SN74LVTH16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143K – MAY 1992 – REVISED APRIL 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16245A	96 mA
SN74LVTH16245A	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16245A	48 mA
SN74LVTH16245A	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DGV package	93°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.



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SN54LVTH16245A, SN74LVTH16245A
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS143K – MAY 1992 – REVISED APRIL 1998

recommended operating conditions (see Note 4)

		SN54LVTH16245A		SN74LVTH16245A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		–24		–32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} –0.5 V to 4.8 V
Input voltage range, V_I (see Note 1) –0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O (see Note 2): SN54LVTH16245A 88 mA
SN74LVTH16245A 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16245A 48 mA
SN74LVTH16245A 64 mA
Input clamp current, I_{IK} (V_I < 0) –80 mA
Output clamp current, I_{OK} (V_O < 0) –80 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package 89°C/W
DGV package 83°C/W
DL package 84°C/W
Storage temperature range, T_{stg} –65°C to 150°C

Exposure to absolute maximum ratings for extended periods may affect device reliability.
Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not guaranteed.
Exceeding these limits may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not guaranteed.

NOTES: 1. The input and output voltage range may be exceeded if the input and output clamp current ratings are observed.
2. This current flows only when the output is in the high state and V_O > V_{CC}.
3. The package thermal impedance is calculated in accordance with JEDEC 81.

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3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16245A			SN74LVTH16245A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
		$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2						
		$V_{CC} = 3 \text{ V}$, $I_{OH} = -32 \text{ mA}$				2			
V_{OL}		$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$			0.2			0.2	V
		$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 24 \text{ mA}$			0.5			0.5	
		$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.4			0.4	
		$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 32 \text{ mA}$			0.5			0.5	
		$V_{CC} = 3 \text{ V}$, $I_{OL} = 48 \text{ mA}$			0.55				
		$V_{CC} = 3 \text{ V}$, $I_{OL} = 64 \text{ mA}$						0.55	
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$			± 1			± 1	μA
		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			10			10	
	A or B ports‡	$V_{CC} = 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			20			20	
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$			5			1	
		$V_{CC} = 3.6 \text{ V}$, $V_I = 0$			-5			-5	
I_{off}		$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75			75			μA
		$V_{CC} = 3 \text{ V}$, $V_I = 2 \text{ V}$	-75			-75			
I_{OZPU}		$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}^\S		$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$			0.19			0.19	mA
		Outputs high			0.19			0.19	
		Outputs low			5			5	
ΔI_{CC}		$V_{CC} = 3 \text{ V to } 3.6$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i		$V_I = 3 \text{ V or } 0$			4			4	pF
C_{io}		$V_O = 3 \text{ V or } 0$			10			10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC} \text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC} \text{ or GND}$.



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(otherwise noted)

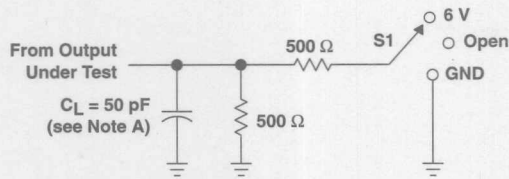
† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

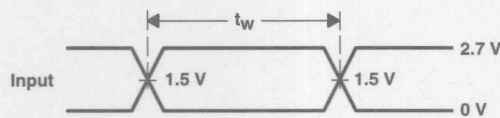
SN54LVTH16245A, SN74LVTH16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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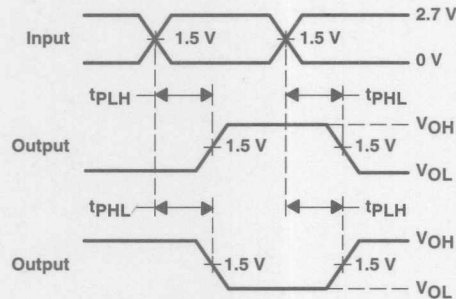
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

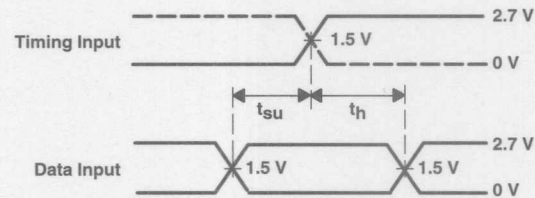


VOLTAGE WAVEFORMS
PULSE DURATION

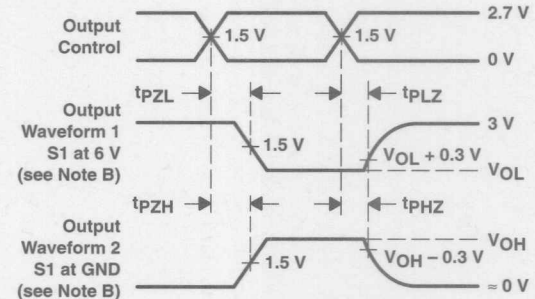


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

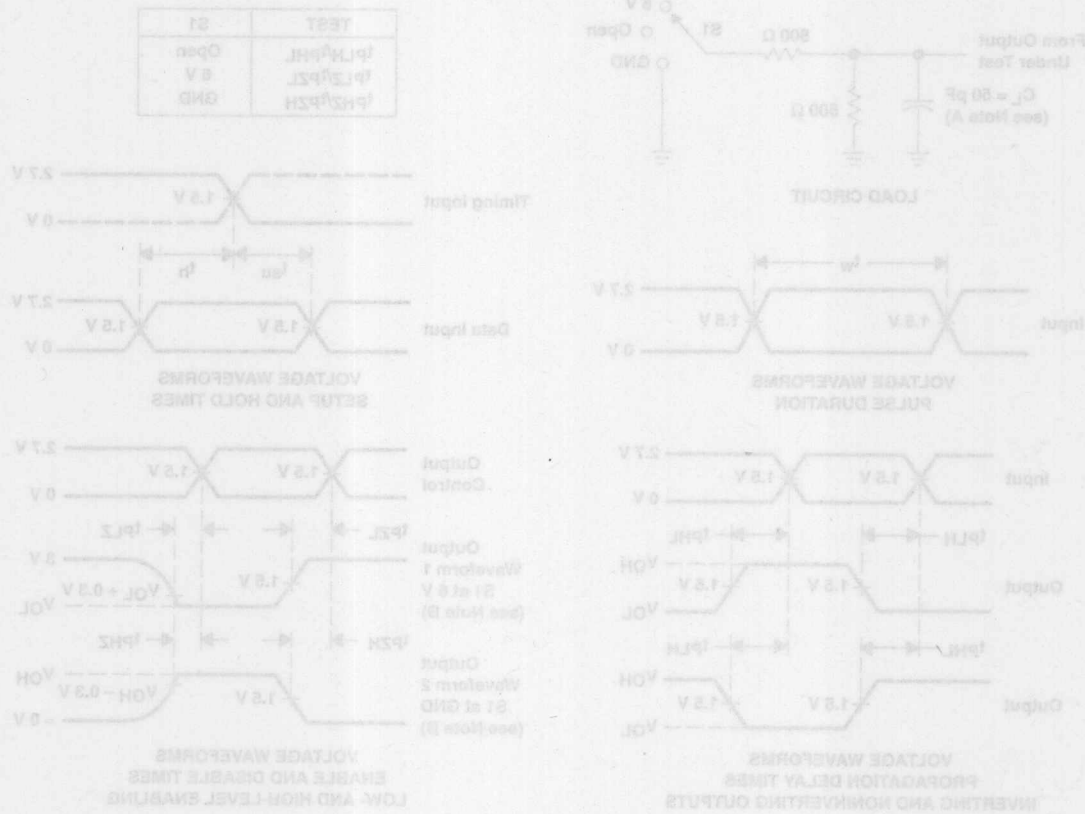


Figure 7. Load Circuit and Voltage Waveforms

NOTES: A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 Ω, VIL = 0.5 V, VIH = 2.7 V.
E. The outputs are measured one at a time with one transition per measurement.

SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- A-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- High-Impedance State During Power Up and Power Down
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162245...WD PACKAGE
SN74LVTH162245...DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	48	1OE
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2OE

description

The 'LVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH162245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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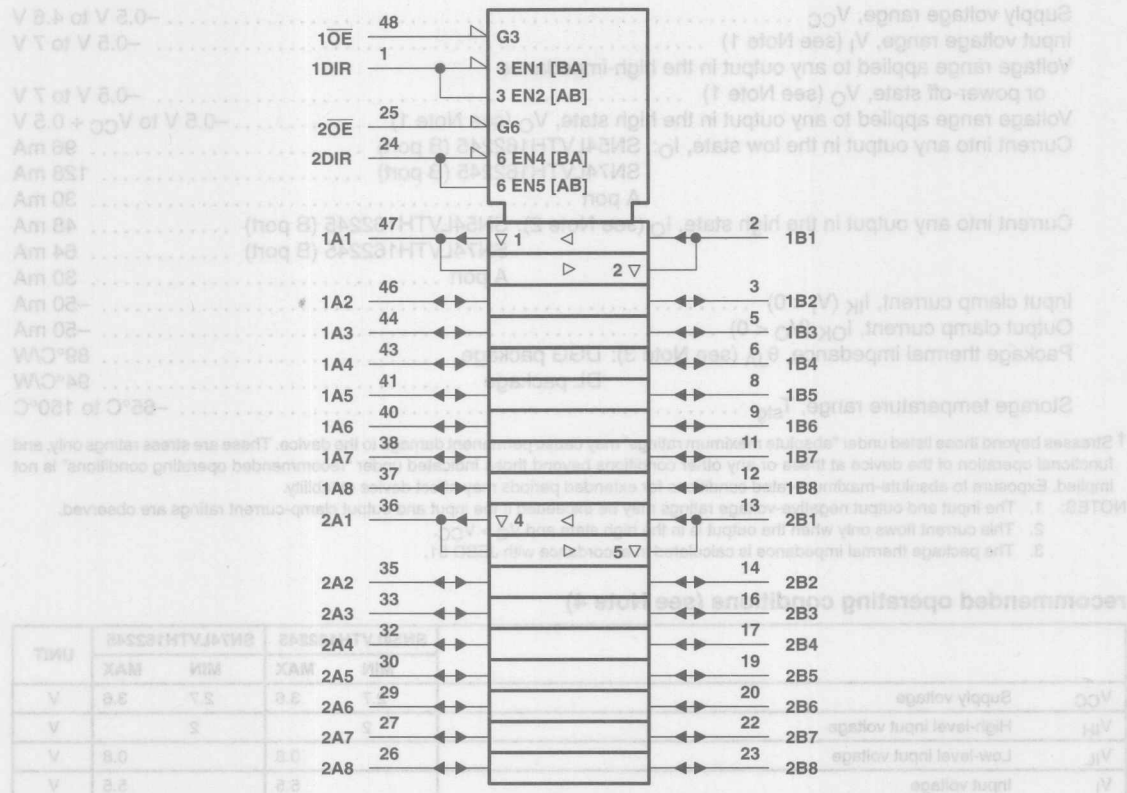


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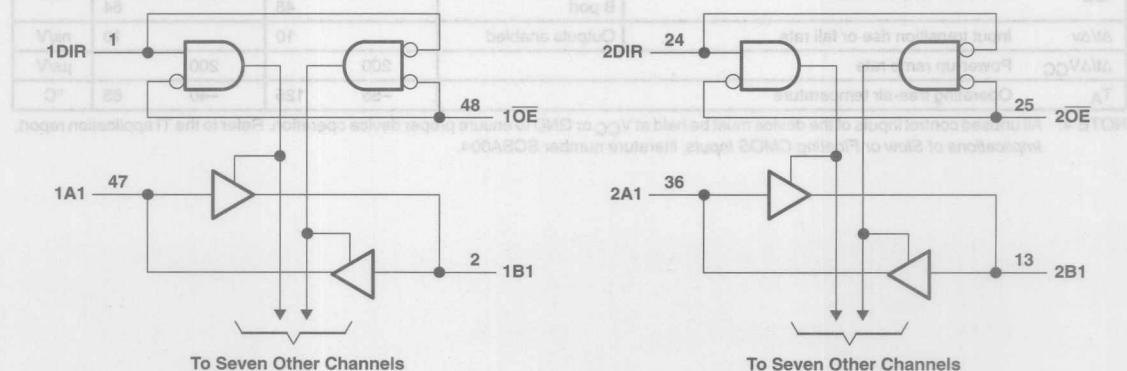
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



**TEXAS
INSTRUMENTS**

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SN54LVTH162245, SN74LVTH162245

3.3-V ABT 16-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH162245 (B port)	96 mA
SN74LVTH162245 (B port)	128 mA
A port	30 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH162245 (B port)	48 mA
SN74LVTH162245 (B port)	64 mA
A port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH162245		SN74LVTH162245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current	A port		–12	–12	mA
		B port		–24	–32	
I_{OL}	Low-level output current	A port		12	12	mA
		B port		48	64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH162245, SN74LVTH162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162245		SN74LVTH162245		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA			-1.2		-1.2	V
V _{OH}	A port	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2		V _{CC} -0.2		V
		V _{CC} = 3 V, I _{OH} = -12 mA		2		2		
	B port	V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2		V _{CC} -0.2		
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4		2.4		
		V _{CC} = 3 V I _{OH} = -24 mA		2				
		I _{OH} = -32 mA				2		
V _{OL}	A port	V _{CC} = 2.7 V to 3.6 V, I _{OL} = 100 μA			0.2		0.2	V
		V _{CC} = 3 V, I _{OL} = 12 mA			0.8		0.8	
	B port	V _{CC} = 2.7 V I _{OL} = 100 μA			0.2		0.2	
		I _{OL} = 24 mA			0.5		0.5	
		I _{OL} = 16 mA			0.4		0.4	
		V _{CC} = 3 V I _{OL} = 32 mA			0.5		0.5	
		I _{OL} = 48 mA			0.55			
		I _{OL} = 64 mA					0.55	
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND			±1		±1	μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V			10		10	
	A or B ports	V _{CC} = 3.6 V V _I = 5.5 V			20		20	
		V _I = V _{CC}			5		5	
		V _I = 0			-10		-10	
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100	μA
I _I (hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA
			V _I = 2 V	-75		-75		
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, \overline{OE} = don't care			±100*		±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, \overline{OE} = don't care			±100*		±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19		0.19	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND			0.3		0.2	mA
C _i		V _I = 3 V or 0			4		4	pF
C _{io}		V _O = 3 V or 0			10		10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF
(unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162245				SN74LVTH162245				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
tPLH	A	B	1	3.5		4	1	2.3	3.3		3.7	ns
tPHL			1	3.5		3.9	1	2.2	3.3		3.5	
tPLH	B	A	1	4.3		5.3	1	2.8	4		4.6	ns
tPHL			1	4.2		4.5	1	2.5	3.4		3.6	
tPZH	\overline{OE}	B	1	4.8		5.9	1	2.8	4.6		5.4	ns
tPZL			1	4.8		5.5	1	3	4.6		5.2	
tPZH	\overline{OE}	A	1	5.5		7.2	1	3.3	5.3		6.3	ns
tPZL			1	5.4		6.4	1	3.3	5.1		5.8	
tPHZ	\overline{OE}	B	1.5	5.5		5.8	1.5	3.8	5.2		5.5	ns
tPLZ			1.5	5.5		5.8	1.5	3.5	5.1		5.4	
tPHZ	\overline{OE}	A	1.5	5.8		6.5	1.5	4	5.6		5.9	ns
tPLZ			1.2	6.3		6.3	1.5	3.8	5.5		5.5	
t _{sk(o)} †								0.5				ns

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

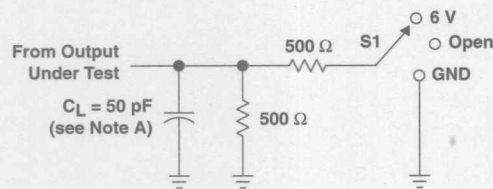
‡ Skew between any two outputs of the same package switching in the same direction

A _{HI}	0.5	0.5	V _I = 0.5 V	V _{CC} = 3.3 V	A or B ports	Inputs
	0	0	V _I = V _{CC}	V _{CC} = 3.3 V		
	-0.5	-0.5	V _I = 0	V _{CC} = 0		
	0.01	0.01	V _I or V _O = 0 to 0.5 V	V _{CC} = 0		
A _{LO}		0.5	V _I = 0.5 V	V _{CC} = 3 V	A or B ports	(if hold)
		-0.5	V _I = -0.5 V			
A _{HI}	0.01	0.01	V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V CE = short-circuited	V _{CC} = 3.3 V		Outputs
A _{LO}	0.01	0.01	V _{CC} = 1.5 V to 0 V, V _O = 0.5 V to 3 V CE = short-circuited	V _{CC} = 3.3 V		Outputs
A _{HI}	0.19	0.19	Outputs high	V _{CC} = 3.3 V I _O = 0 V _I = V _{CC} or GND		
	0	0	Outputs low			
	0.19	0.19	Outputs disabled			
A _{HI}	0.0	0.0	V _{CC} = 3 V to 0.5 V One input at V _{CC} = 0.5 V Other inputs at V _{CC} or GND			
A _{LO}	0	0	V _I = 3 V or 0			
A _{HI}	0	0	V _O = 3 V or 0			

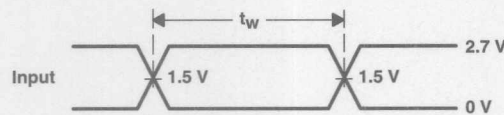
SN54LVTH162245, SN74LVTH162245
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS260J – JUNE 1993 – REVISED – MARCH 1998

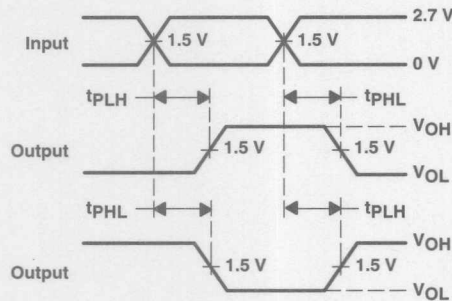
PARAMETER MEASUREMENT INFORMATION



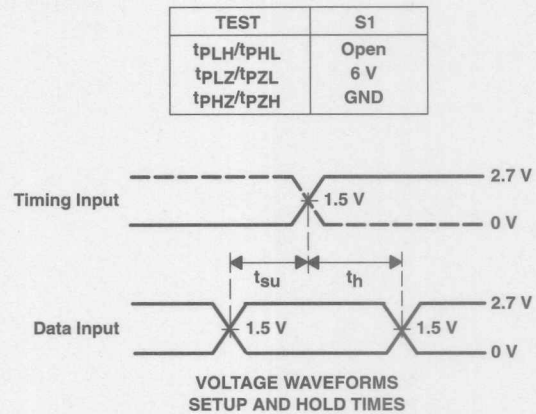
LOAD CIRCUIT



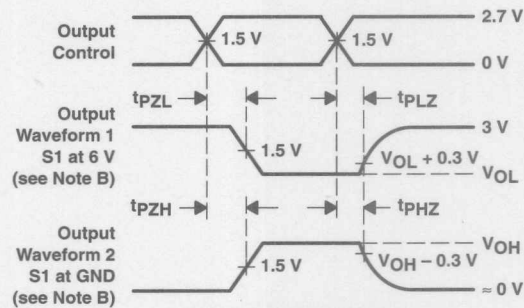
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

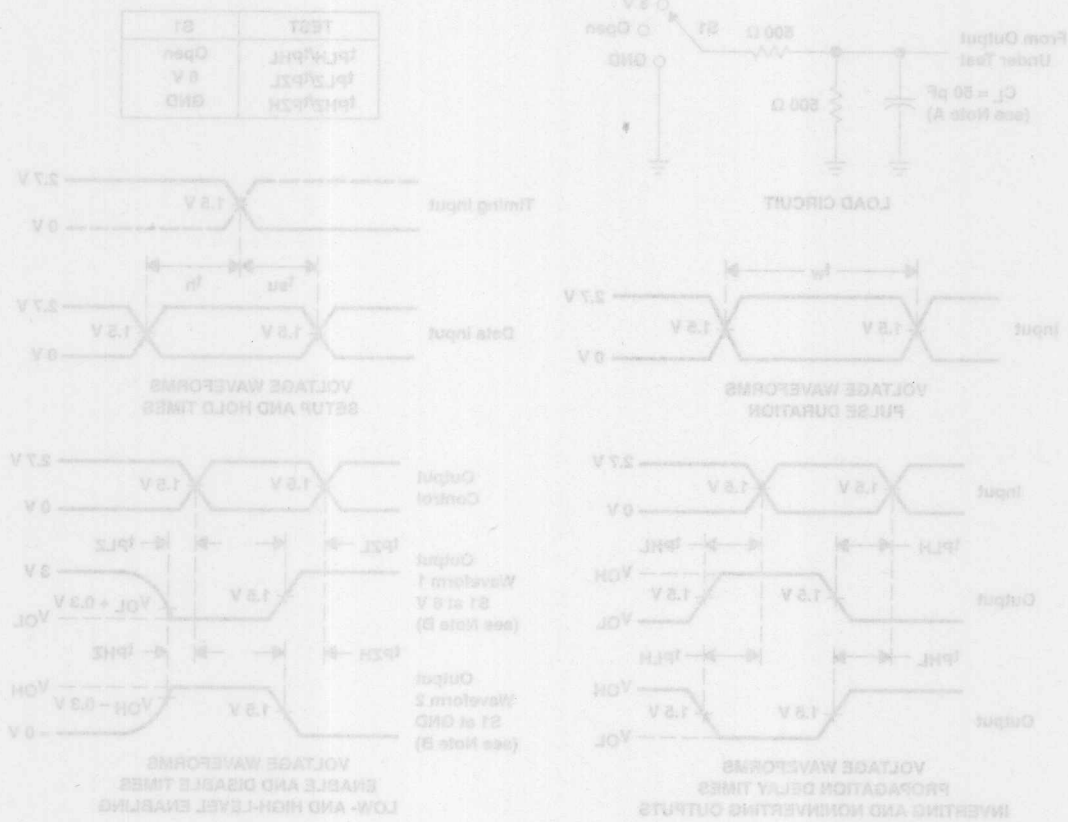


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is low except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, CL = 50 pF, and 2.5 ns rise and fall times.
E. The outputs are measured one at a time with one transition per measurement.

Figure 7. Load Circuit and Voltage Waveforms

SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144J – MAY 1992 – REVISED MARCH – 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16373 ... WD PACKAGE
SN74LVTH16373 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2OE	24	25	2LE

description

The 'LVTH16373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS144J – MAY 1992 – REVISED MARCH – 1998

description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16373 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

The LVTH16373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

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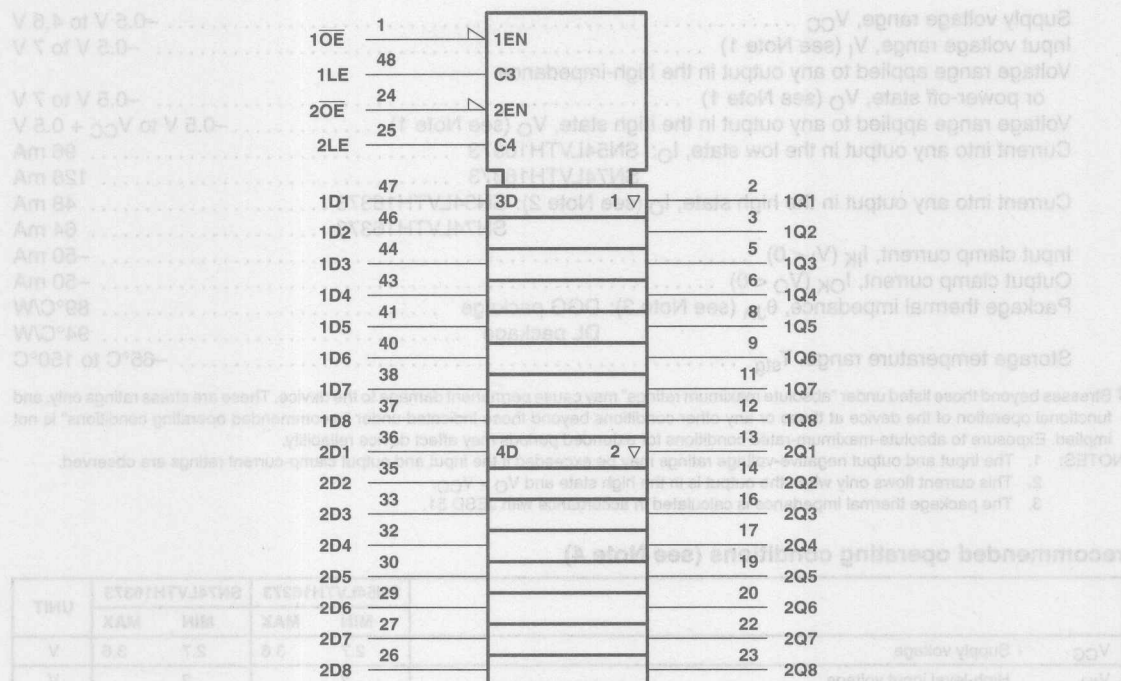


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SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

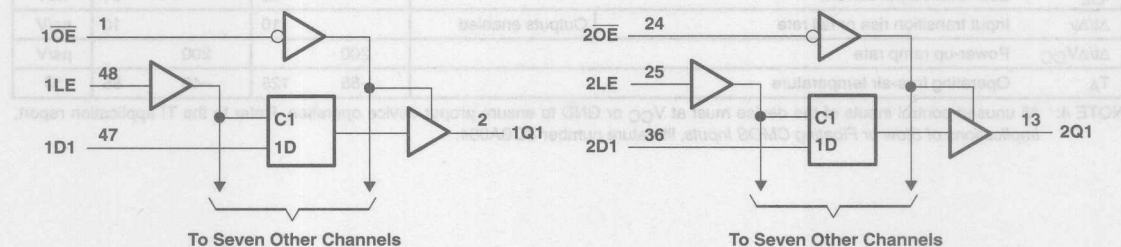
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH16373, SN74LVTH16373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16373	96 mA
SN74LVTH16373	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16373	48 mA
SN74LVTH16373	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51.

recommended operating conditions (see Note 4)

		SN54LVTH16373		SN74LVTH16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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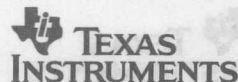
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16373		SN74LVTH16373		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA	-1.2		-1.2		V
V _{OH}		V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4		
		V _{CC} = 3 V	I _{OH} = -24 mA	2		2		
			I _{OH} = -32 mA					
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA	0.2		0.2		V
			I _{OL} = 24 mA	0.5		0.5		
		V _{CC} = 3 V	I _{OL} = 16 mA	0.4		0.4		
			I _{OL} = 32 mA	0.5		0.5		
			I _{OL} = 48 mA	0.55				
			I _{OL} = 64 mA			0.55		
I _I		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	10		10		μA
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND	±1		±1		
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC} V _I = 0	1 -5		1 -5		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA
I _I (hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA
			V _I = 2 V	-75		-75		
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V	5		5		μA
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V	-5		-5		μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*		±100		μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*		±100		μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.19		0.19		mA
			Outputs low	5		5		
			Outputs disabled	0.19		0.19		
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA
C _i		V _I = 3 V or 0		3		3		pF
C _o		V _O = 3 V or 0		9		9		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH16373, SN74LVTH16373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

THU	SN54LVTH16373			SN54LVTH16373			SN54LVTH16373				SN74LVTH16373				UNIT
	V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V			V _{CC} = 3.3 V ± 0.3 V				V _{CC} = 2.7 V				
	MIN	MAX		MIN	MAX		MIN	MAX		MIN	MAX				
t _w	Pulse duration, LE high						3	3	3	3	3	3	ns		
t _{su}	Setup time, data before LE↓						2	2	1	0.6	0.6	0.6	ns		
t _h	Hold time, data after LE↓						3	3.3	1	1.1	1.1	1.1	ns		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16373				SN74LVTH16373				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	D	Q	1.4	4.5		5.2	1.5	2.7	3.8		4.2	ns
t _{PHL}			1.4	4.4		4.8	1.5	2.5	3.6		4	
t _{PLH}	LE	Q	1.8	5.5		5.8	2.1	3	4.3		4.8	ns
t _{PHL}			1.8	5.2		5.6	2.1	2.9	4		4	
t _{PZH}	OE	Q	1.4	5.7		6.7	1.5	2.8	4.3		5.1	ns
t _{PZL}			1.4	5.5		6	1.5	2.8	4.3		4.7	
t _{PHZ}	OE	Q	2	6		6.2	2.4	3.5	5		5.4	ns
t _{PLZ}			1.4	5.2		5.6	2	3.2	4.7		4.8	
t _{sk(o)‡}									0.5			ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

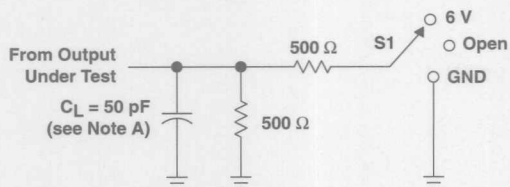
‡ Skew between any two outputs of the same package switching in the same direction



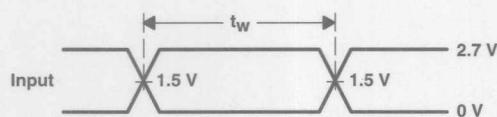
SN54LVTH16373, SN74LVTH16373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS144J – MAY 1992 – REVISED MARCH – 1998

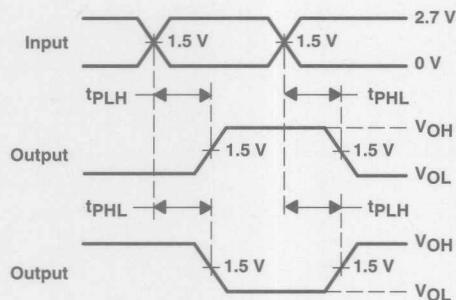
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

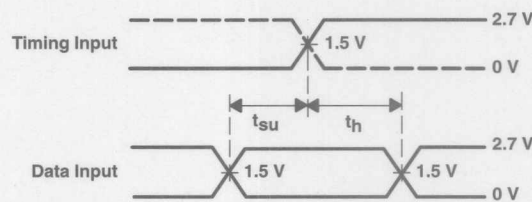


VOLTAGE WAVEFORMS
PULSE DURATION

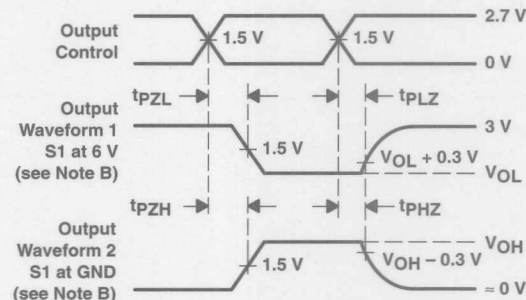


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

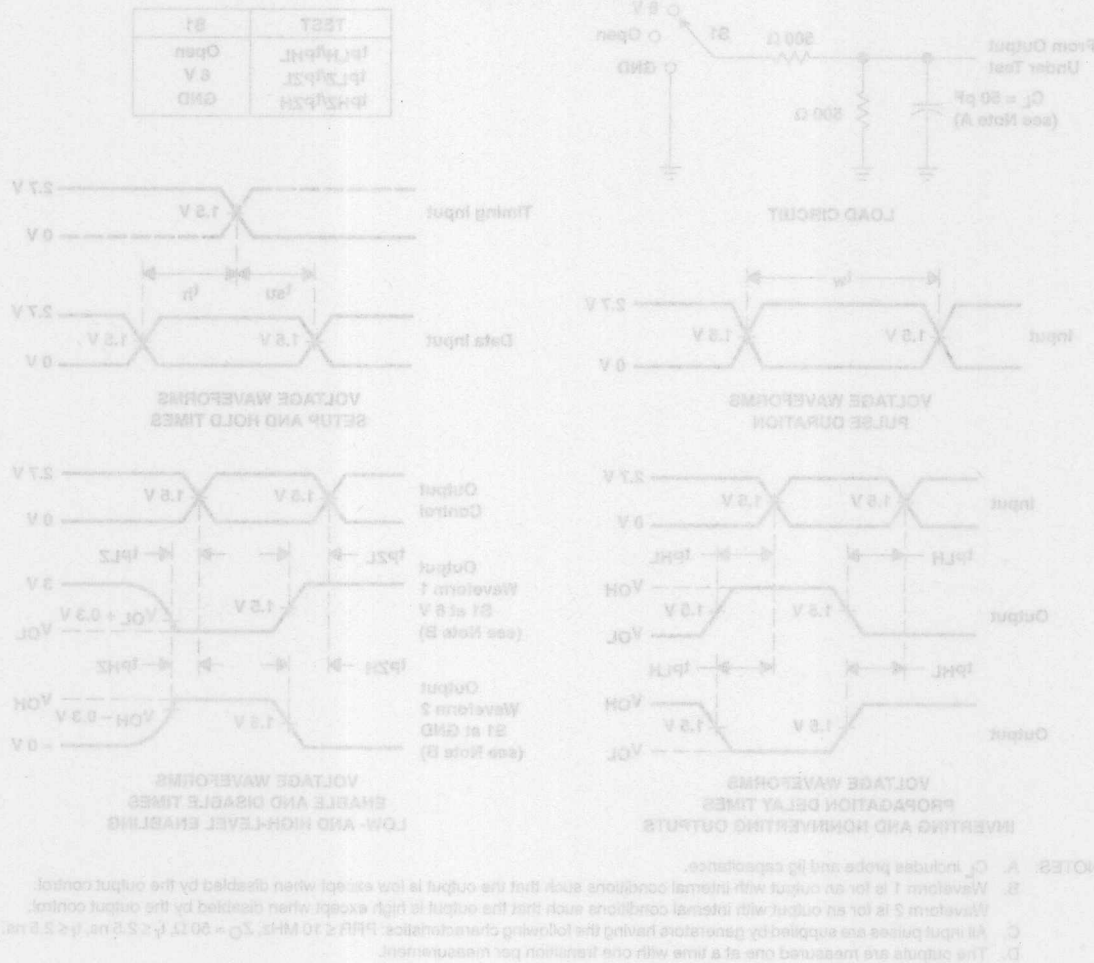


Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCBS2611 – JULY 1993 – REVISED MARCH 1998

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162373 ... WD PACKAGE
SN74LVTH162373 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V _{CC}	7	42	V _{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V _{CC}	18	31	V _{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2OE	24	25	2LE

description

The 'LVTH162373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

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SN54LVTH162373, SN74LVTH162373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

SCBS2611 – JULY 1993 – REVISED MARCH 1998

description (continued)

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH162373 is characterized for operation from -40°C to 85°C .

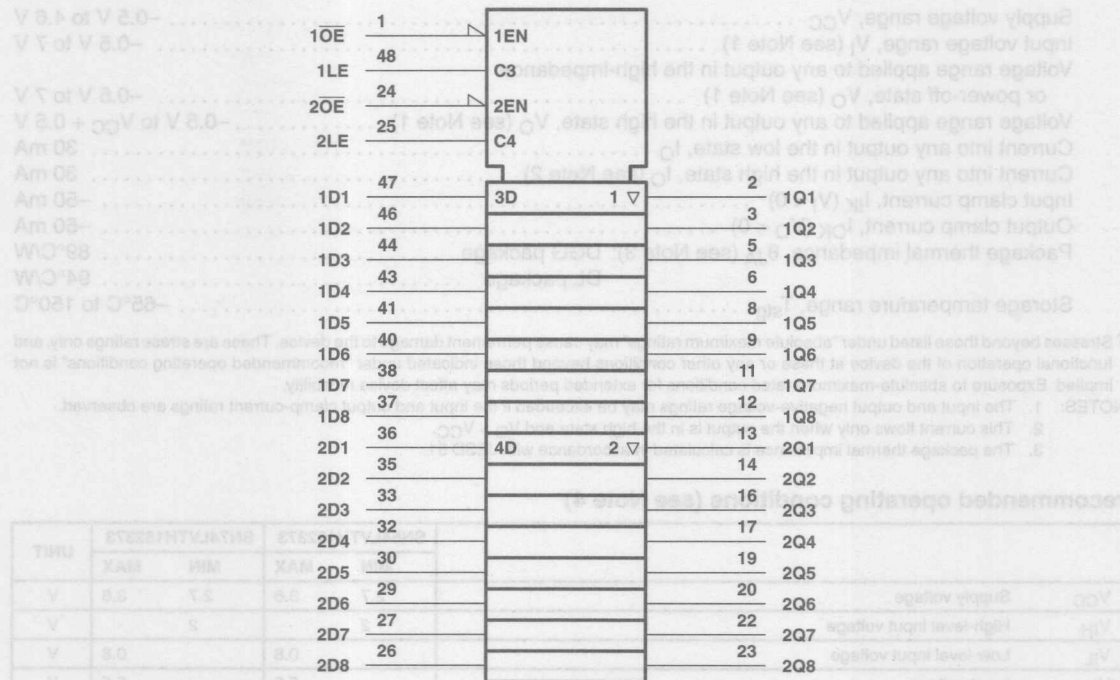
FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

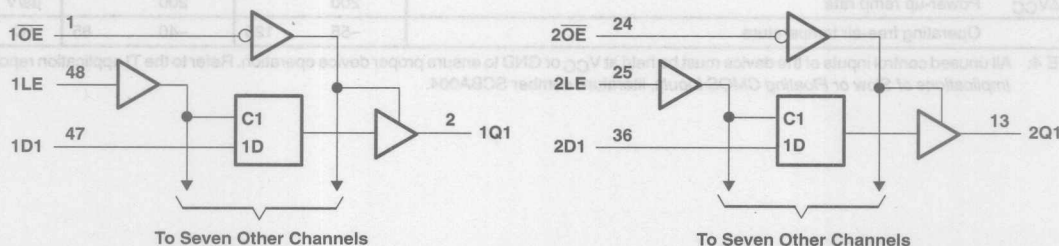
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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SN54LVTH162373, SN74LVTH162373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH162373		SN74LVTH162373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–12		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta V/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta V/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH162373, SN74LVTH162373 3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162373		SN74LVTH162373		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2	-1.2	V
V _{OH}		V _{CC} = 3 V,	I _{OH} = -12 mA	2		2		V
V _{OL}		V _{CC} = 3 V,	I _{OL} = 12 mA			0.8	0.8	V
I _I		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10	10	μA
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1	±1	
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}			1	1	
			V _I = 0			-5	-5	
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V				±100	μA
I _I (hold)	A inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA
			V _I = 2 V	-75		-75		
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5	5	μA
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			-5	-5	μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care				±100*	±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care				±100*	±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			0.19	0.19	mA
			Outputs low			5	5	
			Outputs disabled			0.19	0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2	0.2	mA
C _i		V _I = 3 V or 0				3	3	pF
C _O		V _O = 3 V or 0				9	9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH162373				SN74LVTH162373				UNIT
		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration, LE high	3		3		3		3		ns
t_{SU}	Setup time, data before LE↓	1.3		0.6		1		0.6		ns
t_h	Hold time, data after LE↓	1		1.1		1		1.1		ns



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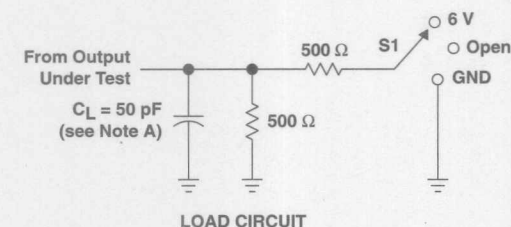
‡ Skew between any two outputs of the same package switching in the same direction

‡ Skew between any two outputs of the same package switching in the same direction

SN54LVTH162373, SN74LVTH162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

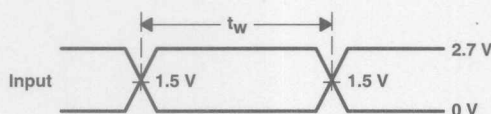
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PARAMETER MEASUREMENT INFORMATION

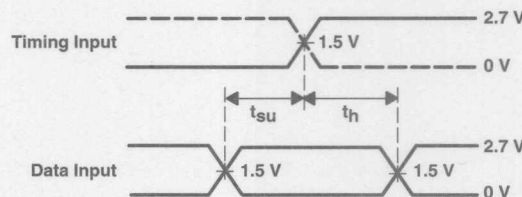


LOAD CIRCUIT

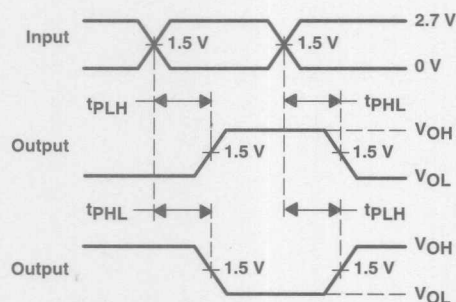
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



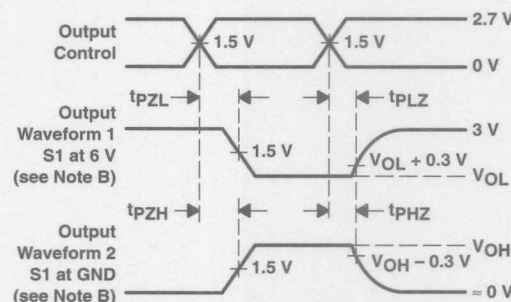
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16374 ... WD PACKAGE
SN74LVTH16374 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	1CLK
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2OE	24	25	2CLK

description

The 'LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH16374, SN74LVTH16374 **3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS** **WITH 3-STATE OUTPUTS**

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description (continued)

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16374 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

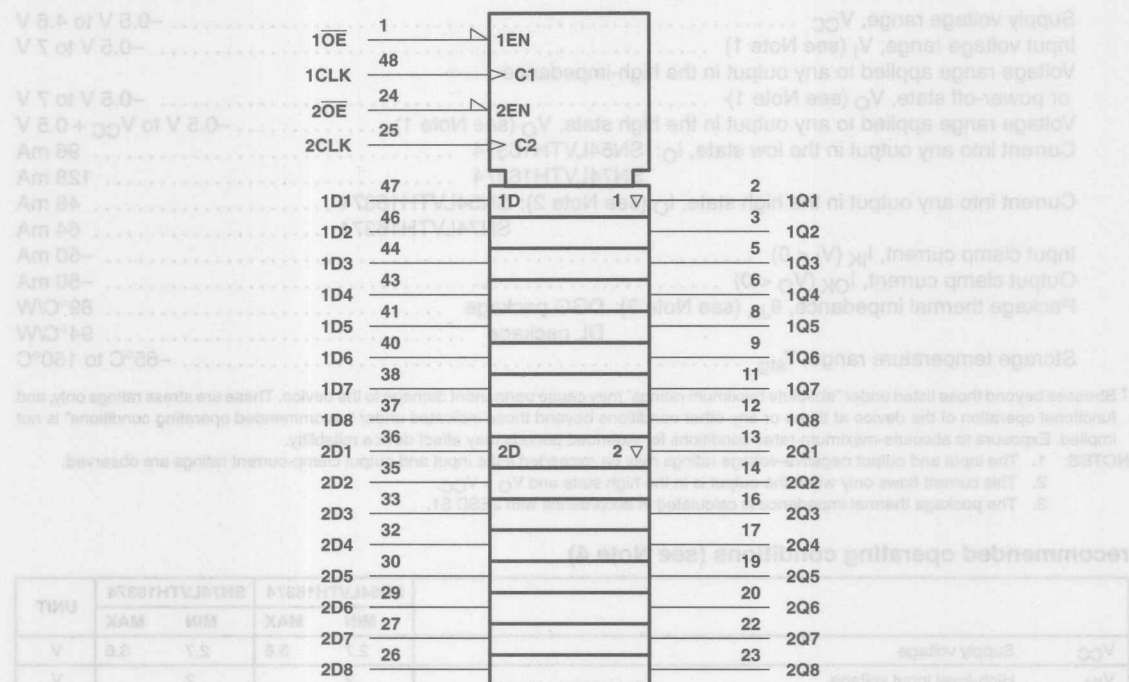
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

The LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

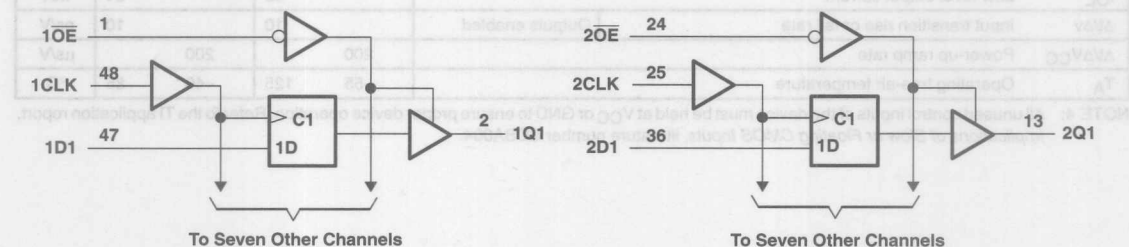
SCBS145K - MAY 1992 - REVISED APRIL 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH16374, SN74LVTH16374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16374	96 mA
SN74LVTH16374	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16374	48 mA
SN74LVTH16374	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16374		SN74LVTH16374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN54LVTH16374, SN74LVTH16374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16374			SN74LVTH16374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			
	$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7 \text{ V}$			0.2			0.2	V
				0.5			0.5	
				0.4			0.4	
	$V_{CC} = 3 \text{ V}$			0.5			0.5	
				0.55				
							0.55	
I_I	Control inputs	$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$		10			10	μA
		$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$		± 1			± 1	
	Data inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC}$		1			1	
		$V_{CC} = 3.6 \text{ V}$, $V_I = 0$		-5			-5	
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75		75			μA
		$V_{CC} = 3 \text{ V}$, $V_I = 2 \text{ V}$	-75		-75			
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $OE = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $OE = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3 \text{ V or } 0$			3			3	pF
C_o	$V_O = 3 \text{ V or } 0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



SN54LVTH16374, SN74LVTH16374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	SN54LVTH16374		SN74LVTH16374		UNIT						
	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		3		3		3		3		ns
t _{su}	Setup time, data before CLK↑		High or low		2.9		3.3		1.8		ns
t _h	Hold time, data after CLK↑		High or low		0.8		0.2		0.8		ns

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16374				SN74LVTH16374				UNIT
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f _{max}			160		160		160		160		MHz
t _{PLH}	CLK	Q	1.4	5.6	6.2		1.9	3	4.5	5.2	ns
t _{PHL}			1.7	4.8	5		2.1	2.9	4	4.2	
t _{PZH}	OE	Q	1	5.6	6.4		1.5	2.8	4.5	5.4	ns
t _{PZL}			1.4	5.5	6.2		1.5	2.8	4.4	5	
t _{PHZ}	OE	Q	1	6.4	6.9		2.4	3.5	5	5.4	ns
t _{PLZ}			1.7	5	5.2		2	3.2	4.6	4.8	
t _{sk(o)} †							0.5				ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Skew between any two outputs of the same package switching in the same direction

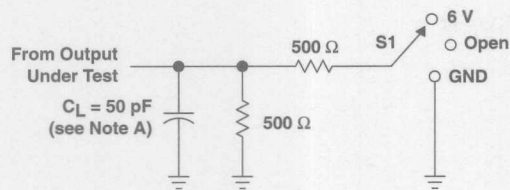


SN54LVTH16374, SN74LVTH16374

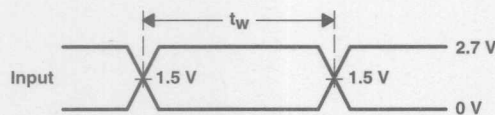
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145K - MAY 1992 - REVISED APRIL 1998

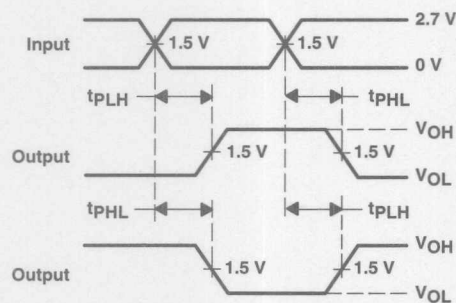
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

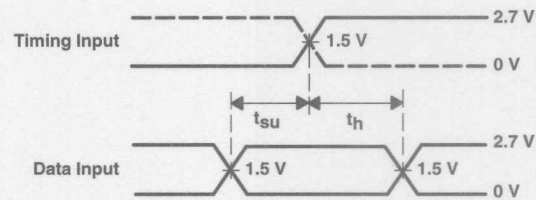


VOLTAGE WAVEFORMS
PULSE DURATION

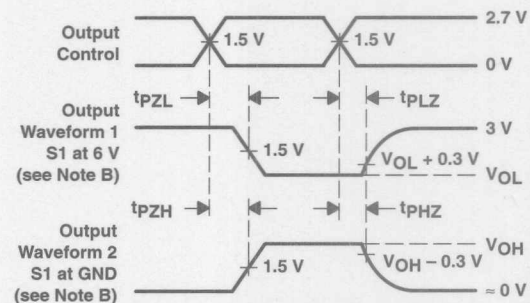


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

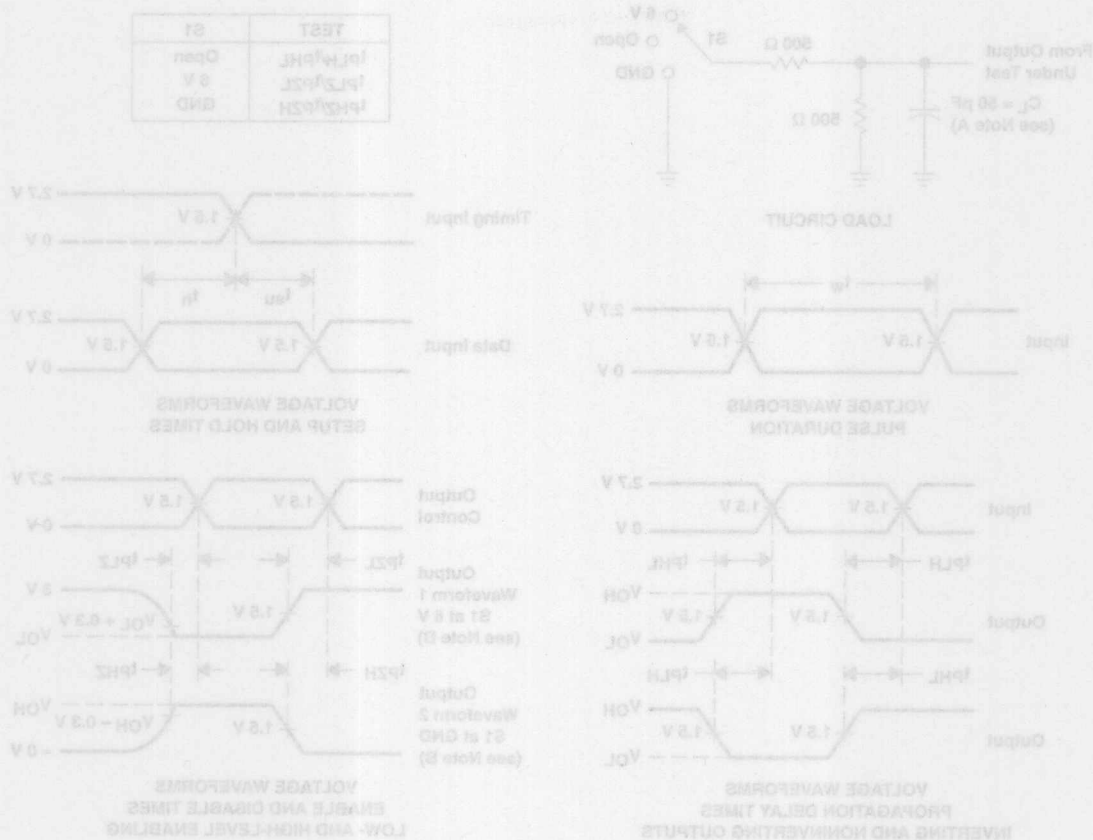


Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_0 \leq 20 \Omega$, $r_s \leq 2.5 \text{ ns}$, $t_r \leq 2.5 \text{ ns}$.
E. The outputs are measured one at a time with one transition per measurement.

SN54LVTH162374, SN74LVTH162374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS262H - JULY 1993 - REVISED APRIL 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162374 . . . WD PACKAGE
SN74LVTH162374 . . . DGG OR DL PACKAGE
(TOP VIEW)


1OE	1	48	1CLK
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2OE	24	25	2CLK

description

The 'LVTH162374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH162374, SN74LVTH162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

WITH 3-STATE OUTPUTS

SCBS262H - JULY 1993 - REVISED APRIL 1998

description (continued)

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH162374 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH162374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

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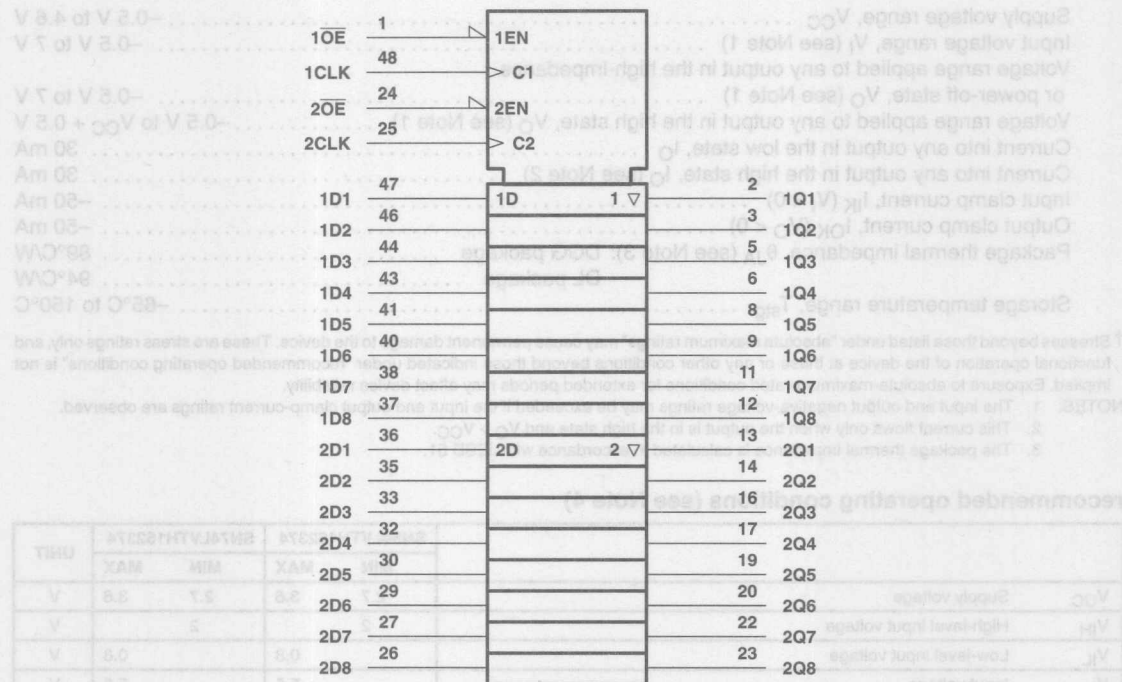
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SN54LVTH162374, SN74LVTH162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

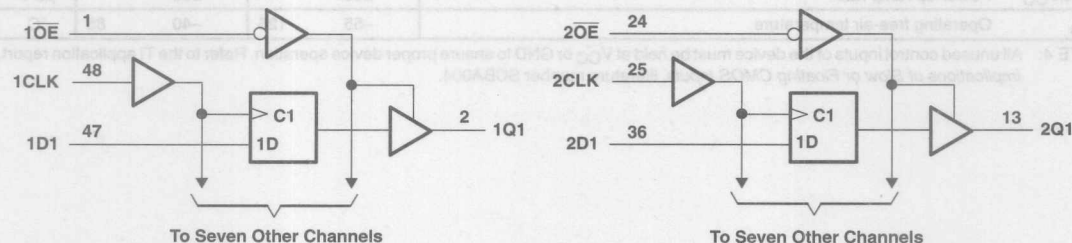
SCBS262H - JULY 1993 - REVISED APRIL 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



SN54LVTH162374, SN74LVTH162374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS262H – JULY 1993 – REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. This current flows only when the output is in the high state and $V_O > V_{CC}$.

3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH162374		SN74LVTH162374		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–12		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVTH162374, SN74LVTH162374 **3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS** **WITH 3-STATE OUTPUTS**

SCBS262H – JULY 1993 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH162374			SN74LVTH162374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 3\text{ V}$, $I_{OH} = -12\text{ mA}$	2			2			V
V_{OL}	$V_{CC} = 3\text{ V}$, $I_{OL} = 12\text{ mA}$			0.8			0.8	V
I_I	$V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$			10			10	
	Control inputs $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$			±1			±1	μA
	Data inputs $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ $V_I = 0$			1 -5			1 -5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						±100	μA
$I_I(\text{hold})$	Data inputs $V_{CC} = 3\text{ V}$			75			75	μA
				-75			-75	
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$			±100*			±100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$			±100*			±100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19	0.19			mA
		Outputs low		5	5			
		Outputs disabled		0.19	0.19			
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or }0$			3			3	pF
C_o	$V_O = 3\text{ V or }0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH162374				SN74LVTH162374				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		160		160		160		160		MHz
t _w	Pulse duration, CLK high or low		3		3.3		3		3		ns
t _{su}	Setup time, data before CLK↑	High or low	2.8		3.2		1.8		2		ns
t _h	Hold time, data after CLK↑	High or low	1.2		0.5		0.8		0.1		ns



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(b) (if not otherwise noted)

[illegible]

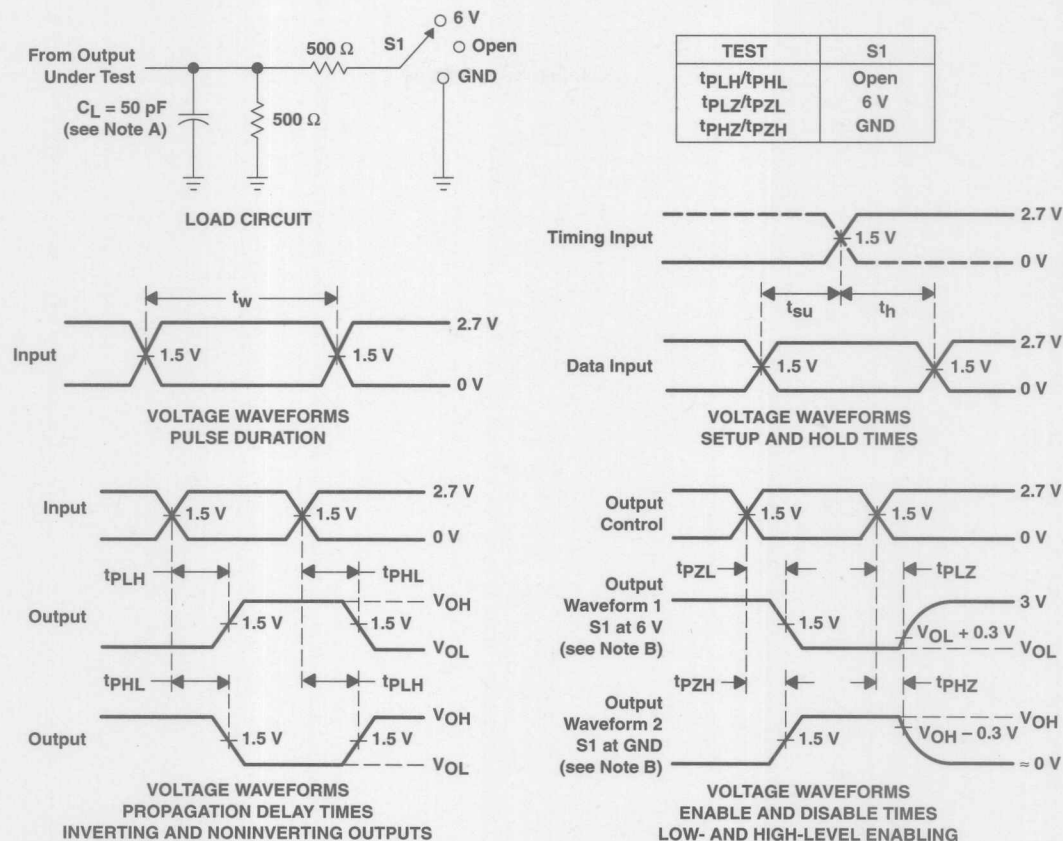
‡ Skew between any two outputs of the same package switching in the same direction

‡ Skew between any two outputs of the same package switching in the same direction

SN54LVTH162374, SN74LVTH162374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701B – JULY 1997 – REVISED MARCH 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- UBT™ (Universal Bus Transceiver)** Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16500 ... WD PACKAGE
SN74LVTH16500 ... DGG OR DL PACKAGE
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

PRODUCT PREVIEW

description

The 'LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the high-to-low transition of CLKAB. Output-enable OEAB is active high. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are in the high-impedance state.

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3-97

SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701B – JULY 1997 – REVISED MARCH 1998

description (continued)

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH16500 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16500 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0^{\ddagger}
H	L	L	X	B_0^{\S}

† A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

‡ Output level before the indicated steady-state input conditions were established

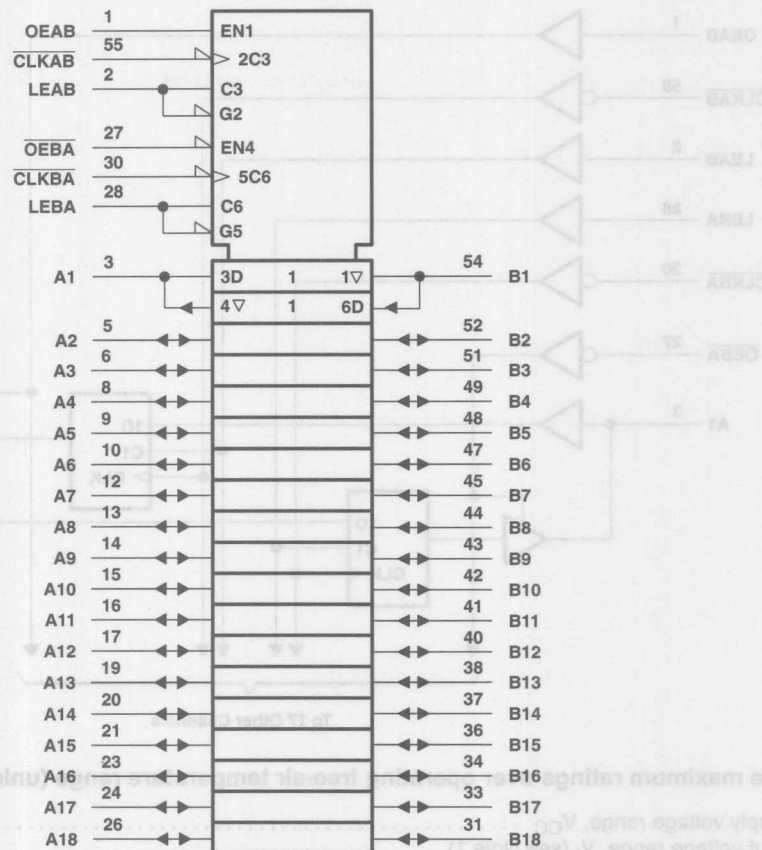
§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

The LVTH16500 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CLKAB}}$ is held at a high or low logic level. If LEAB is low, the A data is stored in the latch on the right-to-low transition of $\overline{\text{CLKAB}}$. Output-enable $\overline{\text{OEAB}}$ is active high. When $\overline{\text{OEAB}}$ is high, the B-port outputs are active. When $\overline{\text{OEAB}}$ is low, the B-port outputs are in the high-impedance state.

SN54LVTH16500, SN74LVTH16500
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS701B - JULY 1997 - REVISED MARCH 1998

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

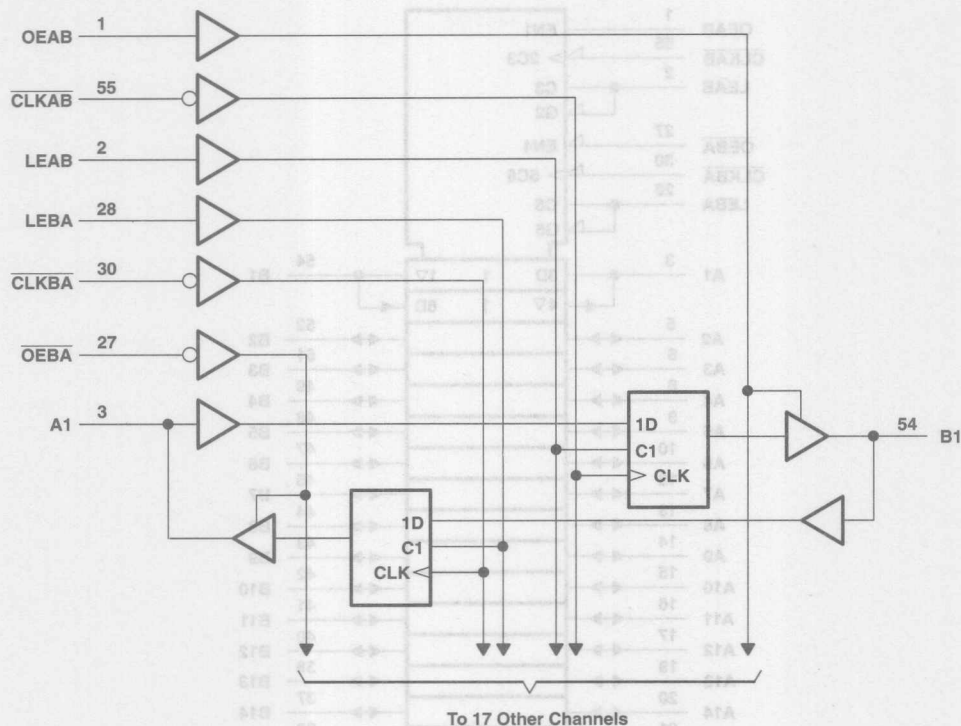
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INSTRUMENTS

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SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS701B – JULY 1997 – REVISED MARCH 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16500	96 mA
SN74LVTH16500	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16500	48 mA
SN74LVTH16500	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.



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WITH 3-STATE OUTPUTS
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recommended operating conditions (see Note 4)

		SN54LVTH16500		SN74LVTH16500		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH16500, SN74LVTH16500
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16500			SN74LVTH16500			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$				-1.2			-1.2	V
V_{OH}		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$		2.4			2.4			
		$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$		2			2			
		$V_{CC} = 3\text{ V}$, $I_{OH} = -32\text{ mA}$								
V_{OL}		$V_{CC} = 2.7\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$				0.2			0.2	V
		$V_{CC} = 2.7\text{ V}$, $I_{OL} = 24\text{ mA}$				0.5			0.5	
		$V_{CC} = 2.7\text{ V}$, $I_{OL} = 16\text{ mA}$				0.4			0.4	
		$V_{CC} = 3\text{ V}$, $I_{OL} = 32\text{ mA}$				0.5			0.5	
		$V_{CC} = 3\text{ V}$, $I_{OL} = 48\text{ mA}$				0.55			0.55	
		$V_{CC} = 3\text{ V}$, $I_{OL} = 64\text{ mA}$							0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$				± 1			± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$				10			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$				20			20	
		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$				5			5	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$				-10			-10	
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$							± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75			75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$		-75			-75			
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$				$\pm 100^*$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$				$\pm 100^*$			± 100	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}^{\S}		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$				0.2			0.2	mA
C_i		$V_I = 3\text{ V or } 0$				3.5			3.5	pF
C_{io}		$V_O = 3\text{ V or } 0$				12			12	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				SN54LVTH16500				SN74LVTH16500				UNIT
				$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		125		150		125		MHz
t_w	Pulse duration			LE high		3.3		3.3		3.3		ns
				CLK high or low		3.3		3.3		3.3		
t_{su}	Setup time			A before CLKAB↓		1.8		1.1		1.8		ns
				B before CLKBA↓		1.9		1.2		1.9		
				A or B before LE↓		CLK high		2.2		1.3		
						CLK low		2.7		1.9		
t_h	Hold time			A or B after CLK↓		1.2		1.2		1.2		ns
				A or B after LE↓		0.9		1.1		0.9		

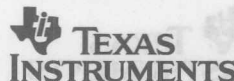
switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16500				SN74LVTH16500				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150		125		150			125		MHz
t_{PLH}	B or A	A or B	1.7	5.8	7		1.7	3	5.4	6.8		ns
t_{PHL}			1.6	6	7.8		1.6	3.2	5.9	7.7		
t_{PLH}	LEBA or LEAB	A or B	2.3	7.3	8.9		2.3	4	7	8.5		ns
t_{PHL}			2.7	8.2	9.8		2.7	4.3	7.9	9.7		
t_{PLH}	$\overline{\text{CLKBA}}$ or $\overline{\text{CLKAB}}$	A or B	2	7.4	8.8		2	4.1	7	8.3		ns
t_{PHL}			2.4	8.1	10		2.4	4.4	7.9	9.9		
t_{PZH}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.2	5.2	6.1		1.2	3	5	5.9		ns
t_{PZL}			1.5	5.9	7		1.5	3	5.8	6.9		
t_{PHZ}	$\overline{\text{OEBA}}$ or OEAB	A or B	2.7	7.7	8.6		2.7	4.6	7.4	8.3		ns
t_{PLZ}			2.8	7.3	7.7		2.8	4.7	6.7	7.2		
$t_{\text{sk(o)}}^{\ddagger}$							0.5				ns	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW

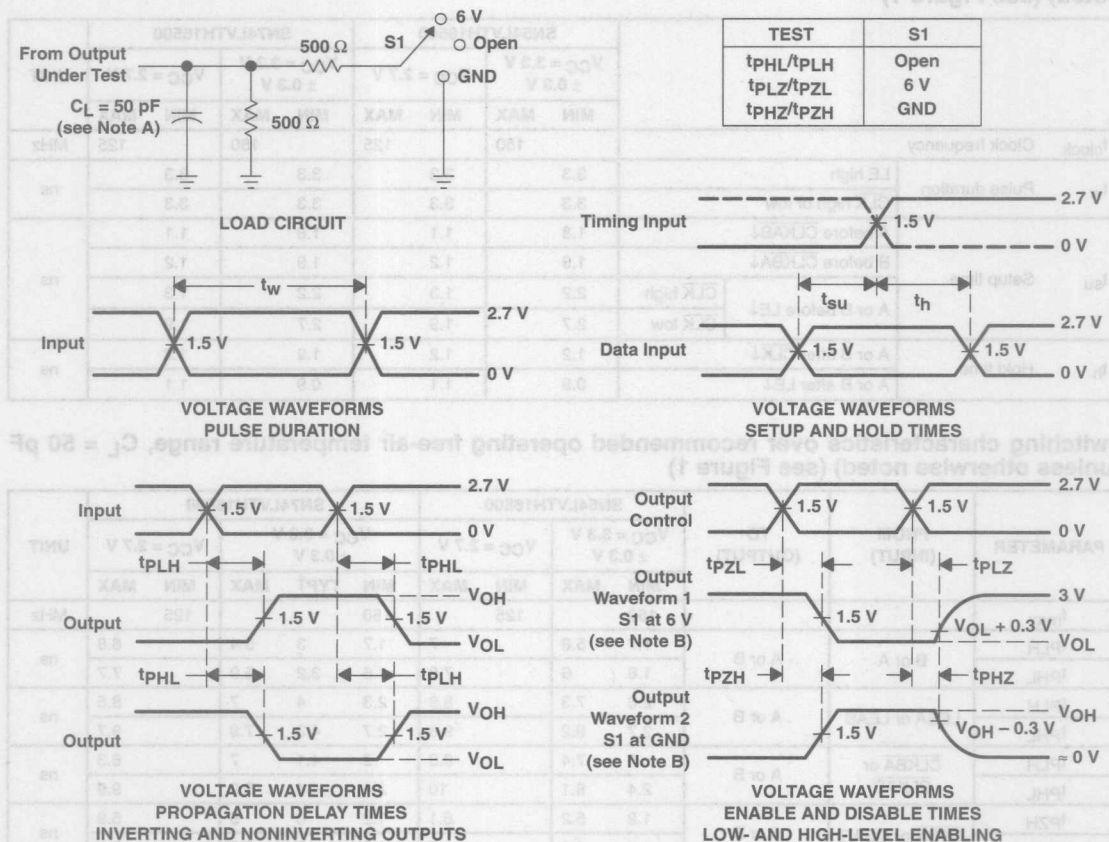


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SN54LVTH16500, SN74LVTH16500 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- *UBT™* (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16501 ... WD PACKAGE
SN74LVTH16501 ... DGG OR DL PACKAGE
(TOP VIEW)

OEAB	1	56	GND
LEAB	2	55	CLKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V_{CC}	7	50	V_{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V_{CC}	22	35	V_{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CLKBA
LEBA	28	29	GND

PRODUCT PREVIEW

description

The LVTH16501 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow in each direction is controlled by output-enable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

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SN54LVTH16501, SN74LVTH16501

3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA. The output enables are complementary (OEAB is active high and $\overline{\text{OEBA}}$ is active low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The SN54LVTH16501 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16501 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B_0^{\ddagger}
H	L	L	X	B_0^{\S}

† A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

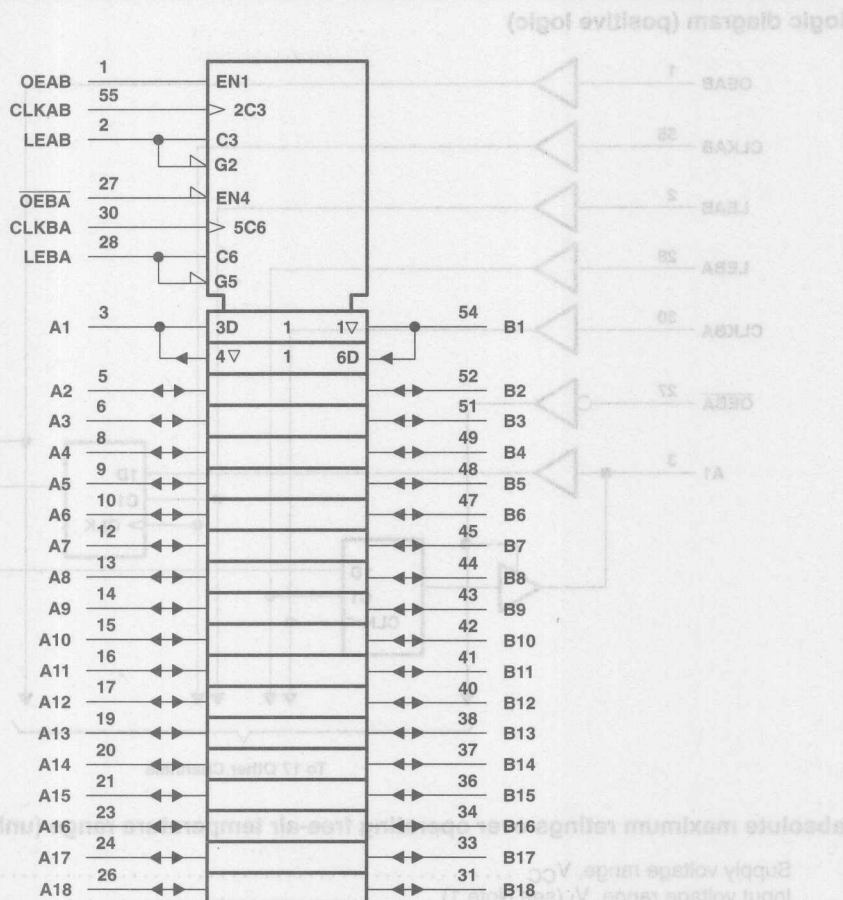
PRODUCT PREVIEW

The LVTH16501 devices are 18-bit universal bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. Data flow in each direction is controlled by output-enable ($\overline{\text{OEBA}}$ and $\overline{\text{OEAB}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the A data is stored in the latch on the low-to-high transition of CLKAB. When OEAB is high, the outputs are active. When OEAB is low, the outputs are in the high-impedance state.

SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

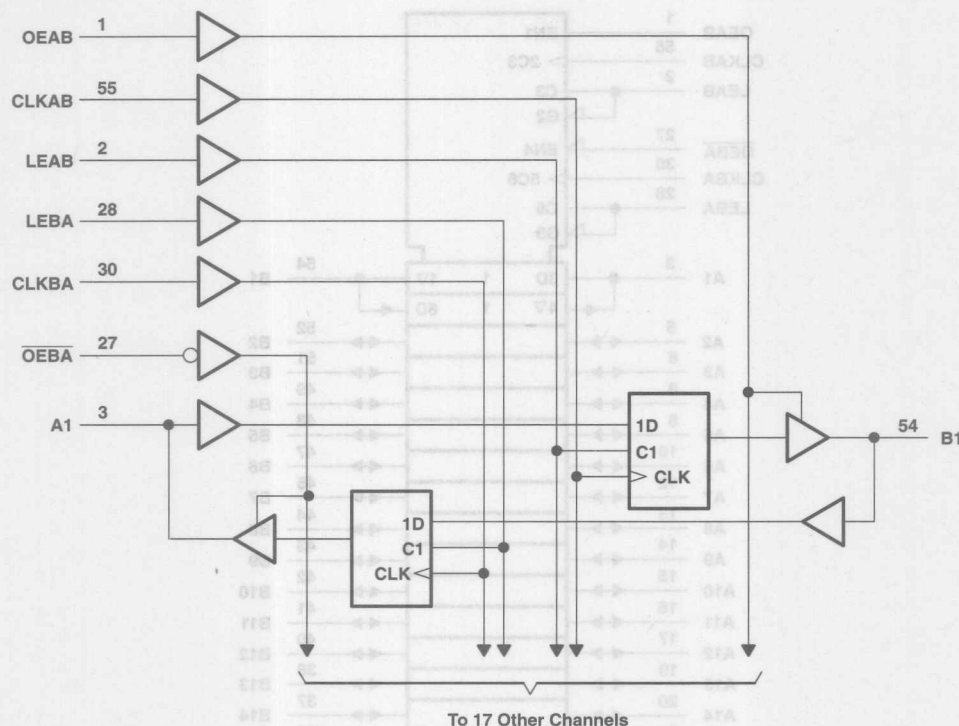


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16501	96 mA
SN74LVTH16501	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16501	48 mA
SN74LVTH16501	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

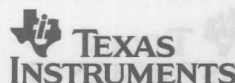
SN54LVTH16501, SN74LVTH16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS
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recommended operating conditions (see Note 4)

		SN54LVTH16501		SN74LVTH16501		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled			10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH16501, SN74LVTH16501
3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16501			SN74LVTH16501			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$, $I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4			V
		$V_{CC} = 3 \text{ V}$, $I_{OH} = -24 \text{ mA}$	2						V
		$I_{OH} = -32 \text{ mA}$				2			V
V_{OL}		$V_{CC} = 2.7 \text{ V}$, $I_{OL} = 100 \mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24 \text{ mA}$			0.5			0.5	V
		$I_{OL} = 16 \text{ mA}$			0.4			0.4	V
		$I_{OL} = 32 \text{ mA}$			0.5			0.5	V
		$V_{CC} = 3 \text{ V}$, $I_{OL} = 48 \text{ mA}$			0.55				V
		$I_{OL} = 64 \text{ mA}$						0.55	V
I_I	Control inputs	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$			± 1			± 1	μA
		$V_{CC} = 0 \text{ or } 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			10			10	
	A or B ports‡	$V_{CC} = 3.6 \text{ V}$, $V_I = 5.5 \text{ V}$			20			20	
		$V_I = V_{CC}$			1			1	
		$V_I = 0$			-5			-5	
I_{off}		$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA
$I_{I(\text{hold})}$	A or B ports	$V_{CC} = 3 \text{ V}$, $V_I = 0.8 \text{ V}$	75			75			μA
		$V_I = 2 \text{ V}$	-75			-75			
I_{OZPU}		$V_{CC} = 0 \text{ to } 1.5 \text{ V}$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5 \text{ V to } 0$, $V_O = 0.5 \text{ V to } 3 \text{ V}$, $\overline{OE}/\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}		$V_{CC} = 3.6 \text{ V}$, $I_O = 0$, $V_I = V_{CC} \text{ or GND}$			0.19			0.19	mA
		Outputs high			5			5	
		Outputs disabled			0.19			0.19	
ΔI_{CC}^\S		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2	mA
C_i		$V_I = 3 \text{ V or } 0$			3.5			3.5	pF
C_{io}		$V_O = 3 \text{ V or } 0$			12			12	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC} \text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC} \text{ or GND}$.

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SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH16501				SN74LVTH16501				UNIT		
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$				
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
f_{clock}	Clock frequency		150		125		150		125		MHz		
t_w	Pulse duration	LE high		3.3		3.3		3.3		3.3		ns	
		CLK high or low		3.3		3.3		3.3		3.3			
t_{su}	Setup time	A before CLKAB↑		1.6		2.1		1.6		2.1		ns	
		B before CLKBA↑		1.6		2.1		1.6		2.1			
		A or B before LE↓	CLK high		3.1		2.7		2.6		1.9		
			CLK low		2.6		2		2		1.3		
t_h	Hold time	A or B after CLK↑		2		2.1		2		2.1		ns	
		A or B after LE↓		1.3		1.2		0.9		1.2			

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16501				SN74LVTH16501				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150		125		150			125		MHz
t_{PLH}	B or A	A or B	1.7	5.4	6.8		1.7	3	5.4	6.8		ns
t_{PHL}			1.6	6	7.8		1.6	3.2	5.9	7.7		
t_{PLH}	LEBA or LEAB	A or B	2.3	7.3	9		2.3	4	7	8.5		ns
t_{PHL}			2.7	8.2	9.8		2.7	4.3	7.9	9.7		
t_{PLH}	CLKBA or CLKAB	A or B	2.5	8.3	9.7		2.5	4.1	7.9	9.2		ns
t_{PHL}			3.5	9.4	10.7		3.5	5.4	8.9	10.4		
t_{PZH}	$\overline{\text{OEBA}}$ or OEAB	A or B	1.2	5.1	6.1		1.2	3	5	5.9		ns
t_{PZL}			1.5	5.9	7		1.5	3	5.8	6.9		
t_{PHZ}	$\overline{\text{OEBA}}$ or OEAB	A or B	2.7	7.5	8.5		2.7	4.6	7.4	8.3		ns
t_{PLZ}			2.8	6.8	7.5		2.8	4.7	6.7	7.2		
$t_{\text{sk(o)}}^{\ddagger}$										0.5		ns

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

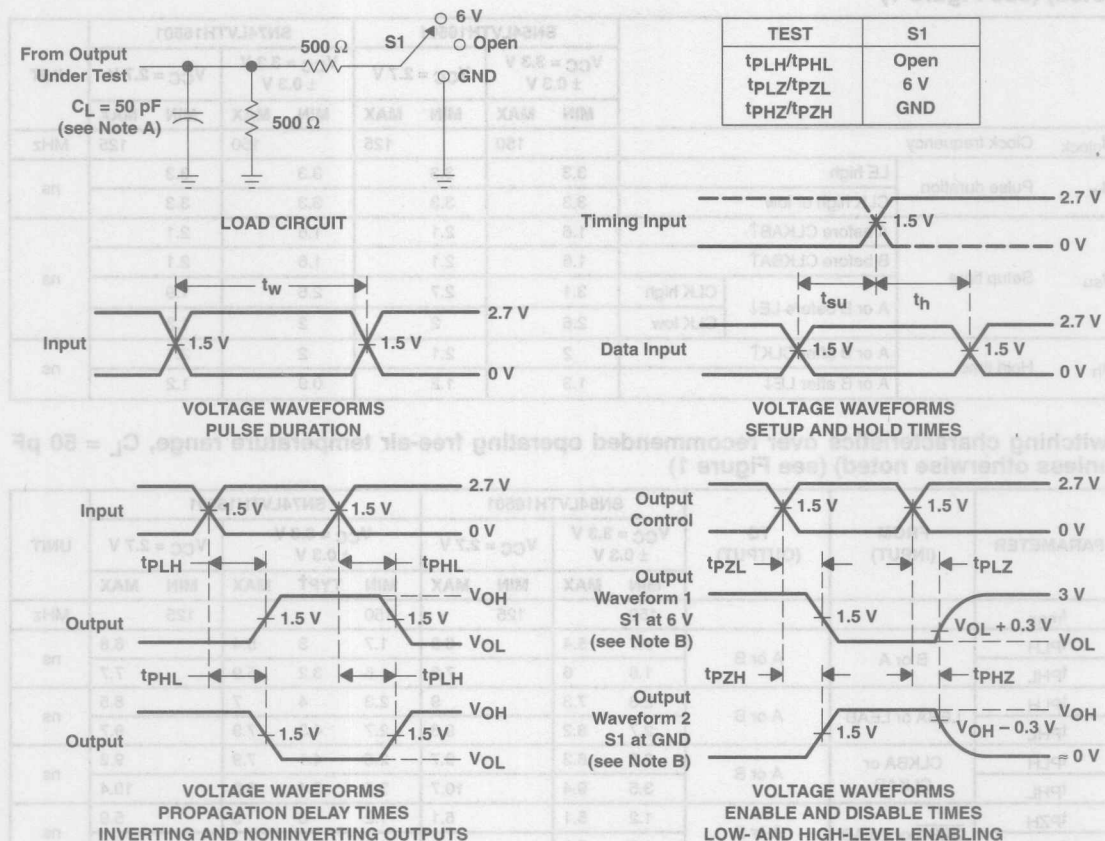
PRODUCT PREVIEW



SN54LVTH16501, SN74LVTH16501 3.3-V ABT 18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS700B – JULY 1997 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16541, SN74LVTH16541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS691C – MAY 1997 – REVISED APRIL 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16541 ... WD PACKAGE
SN74LVTH16541 ... DGG OR DL PACKAGE
(TOP VIEW)

1OE1	1	48	1OE2
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
1Y5	8	41	1A5
1Y6	9	40	1A6
GND	10	39	GND
1Y7	11	38	1A7
1Y8	12	37	1A8
2Y1	13	36	2A1
2Y2	14	35	2A2
GND	15	34	GND
2Y3	16	33	2A3
2Y4	17	32	2A4
V_{CC}	18	31	V_{CC}
2Y5	19	30	2A5
2Y6	20	29	2A6
GND	21	28	GND
2Y7	22	27	2A7
2Y8	23	26	2A8
2OE1	24	25	2OE2

description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable ($1OE1$ and $1OE2$ or $2OE1$ and $2OE2$) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

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SN54LVTH16541, SN74LVTH16541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

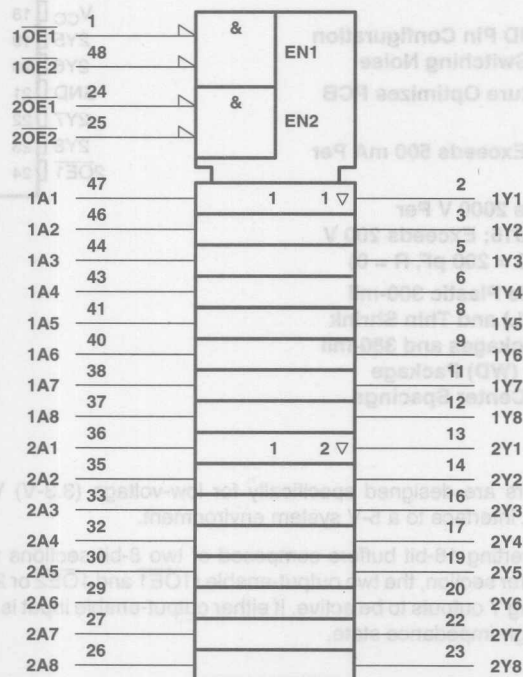
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16541 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16541 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

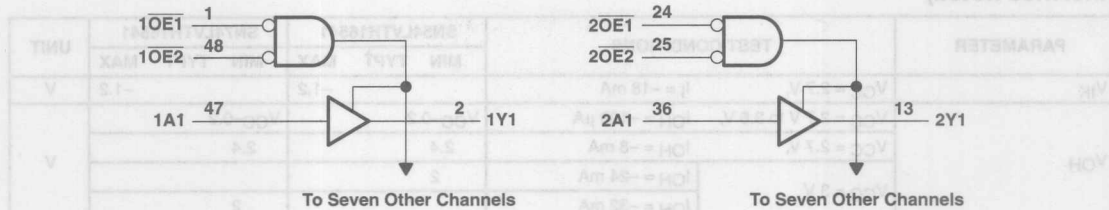


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SN54LVTH16541, SN74LVTH16541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS691C – MAY 1997 – REVISED APRIL 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16541	96 mA
SN74LVTH16541	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16541	48 mA
SN74LVTH16541	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16541		SN74LVTH16541		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**TEXAS
INSTRUMENTS**

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SN54LVTH16541, SN74LVTH16541
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS691C – MAY 1997 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16541			SN74LVTH16541			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
					2			
V_{OL}	$V_{CC} = 2.7\text{ V}$			0.2			0.2	V
				0.5			0.5	
	$V_{CC} = 3\text{ V}$			0.4			0.4	
				0.5			0.5	
				0.55			0.55	
				0.55			0.55	
I_I	$V_{CC} = 0\text{ or } 3.6\text{ V}$, Control inputs		$V_I = 5.5\text{ V}$	10			10	μA
	$V_{CC} = 3.6\text{ V}$, Data inputs		$V_I = V_{CC}\text{ or GND}$	± 1			± 1	
			$V_I = V_{CC}$	1			1	
			$V_I = 0$	-5			-5	
I_{off}	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$							± 100 μA
$I_{I(hold)}$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75		75		μA
			$V_I = 2\text{ V}$	-75		-75		
I_{OZH}	$V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$			5			5	μA
I_{OZL}	$V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$			-5			-5	μA
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, $\overline{OE} = \text{don't care}$			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\ddagger	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			4			4	pF
C_o	$V_O = 3\text{ V or } 0$			9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

I_{OH}	High-level output current	mA	10
I_{OL}	Low-level output current	mA	10
t_{PLH}	Propagation delay from low to high	nA	10
t_{PLZ}	Propagation delay from low to high-Z	nA	10
t_{PHL}	Propagation delay from high to low	nA	10
t_{PHZ}	Propagation delay from high to high-Z	nA	10
t_{PZL}	Propagation delay from high-Z to low	nA	10
t_{PZH}	Propagation delay from high-Z to high	nA	10
t_{ZLH}	Propagation delay from low to high-Z	nA	10
t_{ZLZ}	Propagation delay from low to high-Z	nA	10
t_{ZHL}	Propagation delay from high to high-Z	nA	10
t_{ZHZ}	Propagation delay from high to high-Z	nA	10

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SN54LVTH16541, SN74LVTH16541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS691C – MAY 1997 – REVISED APRIL 1998

switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16541				SN74LVTH16541				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t _{PLH}	A	Y	1	3.7		4	1	2.4	3.5		3.8	ns
t _{PHL}			1	3.7		4	1	2	3.5		3.8	
t _{PZH}	\overline{OE}	Y	1.1	4.8		5.7	1.2	2.7	4.6		5.5	ns
t _{PZL}			1.1	4.8		5.4	1.2	2.8	4.6		5.2	
t _{PHZ}	\overline{OE}	Y	2.1	6.2		6.5	2.2	4.1	5.9		6.2	ns
t _{PLZ}			1.9	5.7		6	2.2	3.8	5.4		5.5	
t _{sk(o)} ‡									0.5		0.5	ns

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

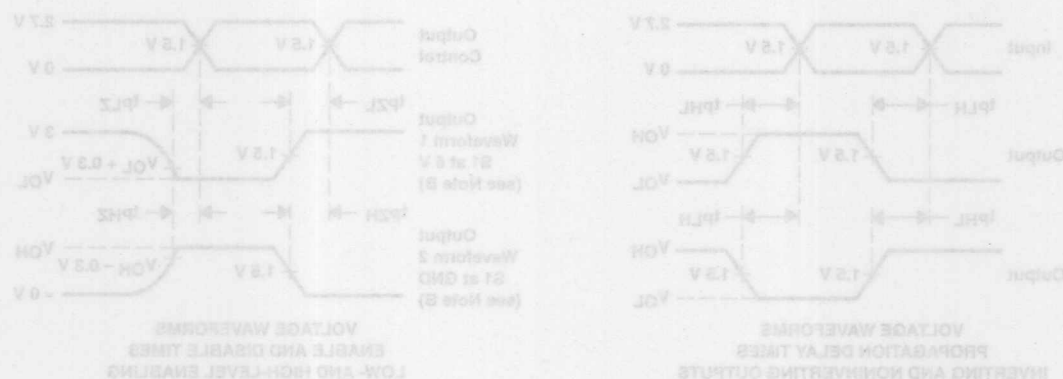


Figure 1. Load Circuit and Voltage Waveforms

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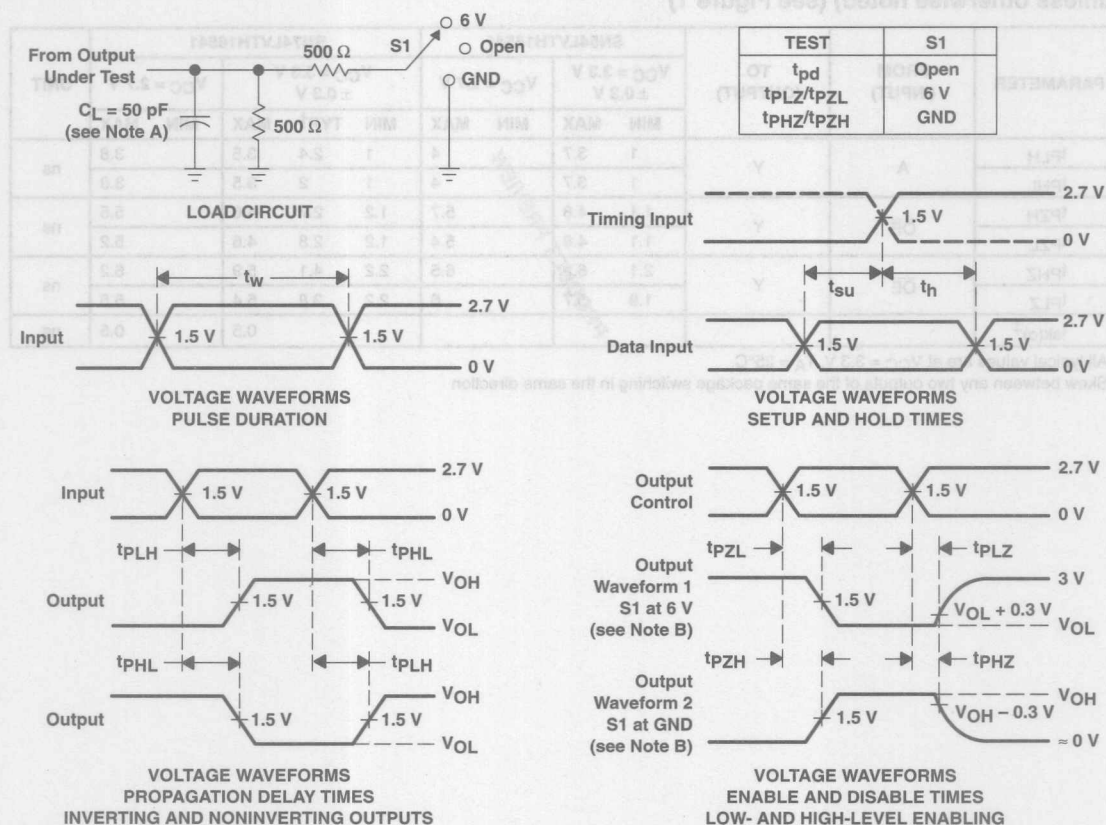


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SN54LVTH16541, SN74LVTH16541
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS691C - MAY 1997 - REVISED APRIL 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH162541, SN74LVTH162541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS690D - MAY 1997 - REVISED MAY 1998

- Members of the Texas Instruments *Widebus™* Family
- Output Ports Have Equivalent 22- Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162541 . . . WD PACKAGE
SN74LVTH162541 . . . DGG OR DL PACKAGE
(TOP VIEW)

1OE1	1	48	1OE2
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
1Y5	8	41	1A5
1Y6	9	40	1A6
GND	10	39	GND
1Y7	11	38	1A7
1Y8	12	37	1A8
2Y1	13	36	2A1
2Y2	14	35	2A2
GND	15	34	GND
2Y3	16	33	2A3
2Y4	17	32	2A4
V_{CC}	18	31	V_{CC}
2Y5	19	30	2A5
2Y6	20	29	2A6
GND	21	28	GND
2Y7	22	27	2A7
2Y8	23	26	2A8
2OE1	24	25	2OE2

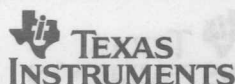
description

These 16-bit buffers/drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices are noninverting 16-bit buffers composed of two 8-bit sections with separate output-enable signals. For either 8-bit buffer section, the two output-enable (1OE1 and 1OE2 or 2OE1 and 2OE2) inputs must be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 8-bit buffer section are in the high-impedance state.

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SN54LVTH162541, SN74LVTH162541 **3.3-V ABT 16-BIT BUFFERS/DRIVERS** **WITH 3-STATE OUTPUTS**

SCBS690D – MAY 1997 – REVISED MAY 1998

description (continued)

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

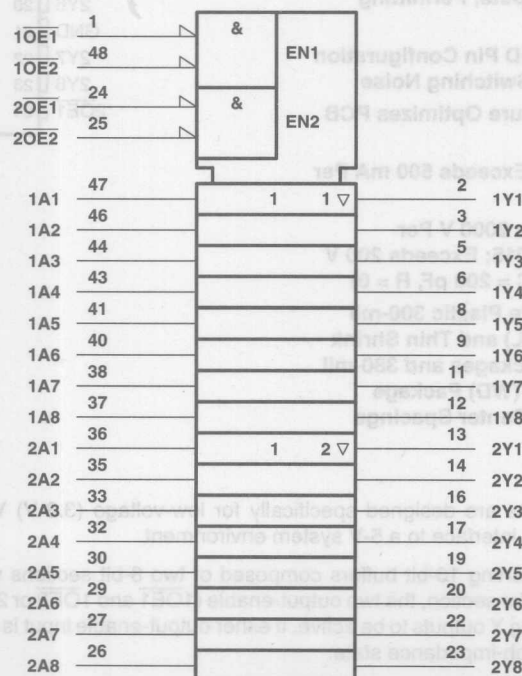
The SN54LVTH162541 is characterized for operation over the full military temperature range of -55°C to 125°C .

The SN74LVTH162541 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†

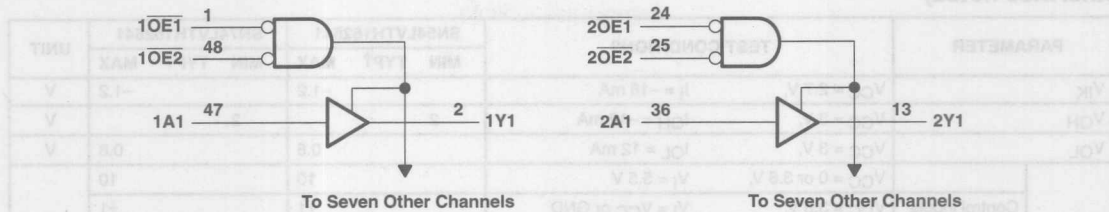


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54LVTH162541, SN74LVTH162541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS690D – MAY 1997 – REVISED MAY 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O	30 mA
Current into any output in the high state, I_O (see Note 2)	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH162541		SN74LVTH162541		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–12		–12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH162541, SN74LVTH162541 **3.3-V ABT 16-BIT BUFFERS/DRIVERS** **WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162541		SN74LVTH162541		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2	-1.2	V
V _{OH}		V _{CC} = 3 V,	I _{OH} = -12 mA	2			2	V
V _{OL}		V _{CC} = 3 V,	I _{OL} = 12 mA			0.8	0.8	V
I _I		V _{CC} = 0 or 3.6 V,	V _I = 5.5 V			10	10	μA
	Control inputs	V _{CC} = 3.6 V,	V _I = V _{CC} or GND			±1	±1	
	Data inputs	V _{CC} = 3.6 V	V _I = V _{CC}			1	1	
			V _I = 0			-5	-5	
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V				±100	μA
I _I (hold)	Data inputs	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA
			V _I = 2 V	-75		-75		
I _{OZH}		V _{CC} = 3.6 V,	V _O = 3 V			5	5	μA
I _{OZL}		V _{CC} = 3.6 V,	V _O = 0.5 V			-5	-5	μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care				±100*	±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care				±100*	±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			0.19	0.19	mA
			Outputs low			5	5	
			Outputs disabled			0.19	0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND				0.2	0.2	mA
C _i		V _I = 3 V or 0				4	4	pF
C _o		V _O = 3 V or 0				9	9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162541				SN74LVTH162541				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	Y	1.1	4.3	4.9		1.2	2.9	4.1	4.7		ns
t _{PHL}			1.1	4.3	4.9		1.2	2.4	4.1	4.7		
t _{PZH}	OE	Y	1.4	5.3	6.3		1.5	3.2	5	6.1		ns
t _{PZL}			1.4	5.1	5.8		1.5	3.3	4.8	5.5		
t _{PHZ}	OE	Y	2.1	6.4	6.4		2.2	4.3	5.9	6.2		ns
t _{PLZ}			2.1	5.7	5.9		2.2	4	5.4	5.5		
t _{sk(o)} §									0.5	0.5		ns

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

§ Skew between any two outputs of the same package switching in the same direction

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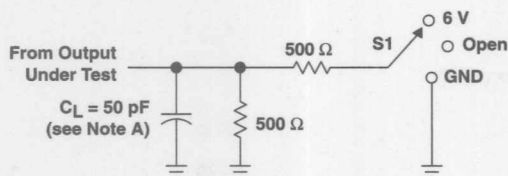


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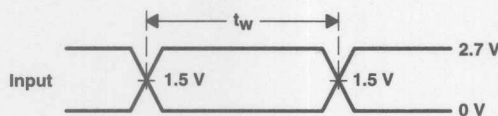
SN54LVTH162541, SN74LVTH162541 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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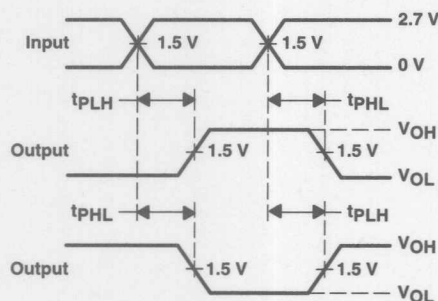
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

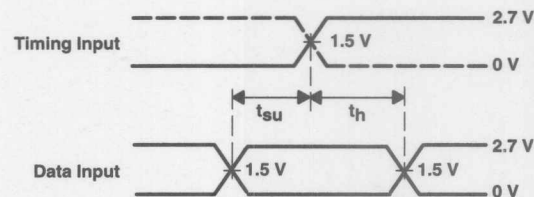


VOLTAGE WAVEFORMS
PULSE DURATION

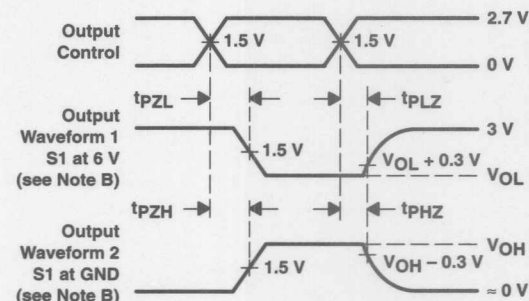


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16543 ... WD PACKAGE
SN74LVTH16543 ... DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1LEAB	2	55	1LEBA
1CEAB	3	54	1CEBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CEAB	26	31	2CEBA
2LEAB	27	30	2LEBA
2OEAB	28	29	2OEBA

description

The 'LVTH16543 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (LEAB or LEBA) and output-enable (OEAB or OEBA) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

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SN54LVTH16543, SN74LVTH16543 **3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS** **WITH 3-STATE OUTPUTS**

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description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†
(each 8-bit section)

INPUTS				OUTPUT B
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^{\ddagger}
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established

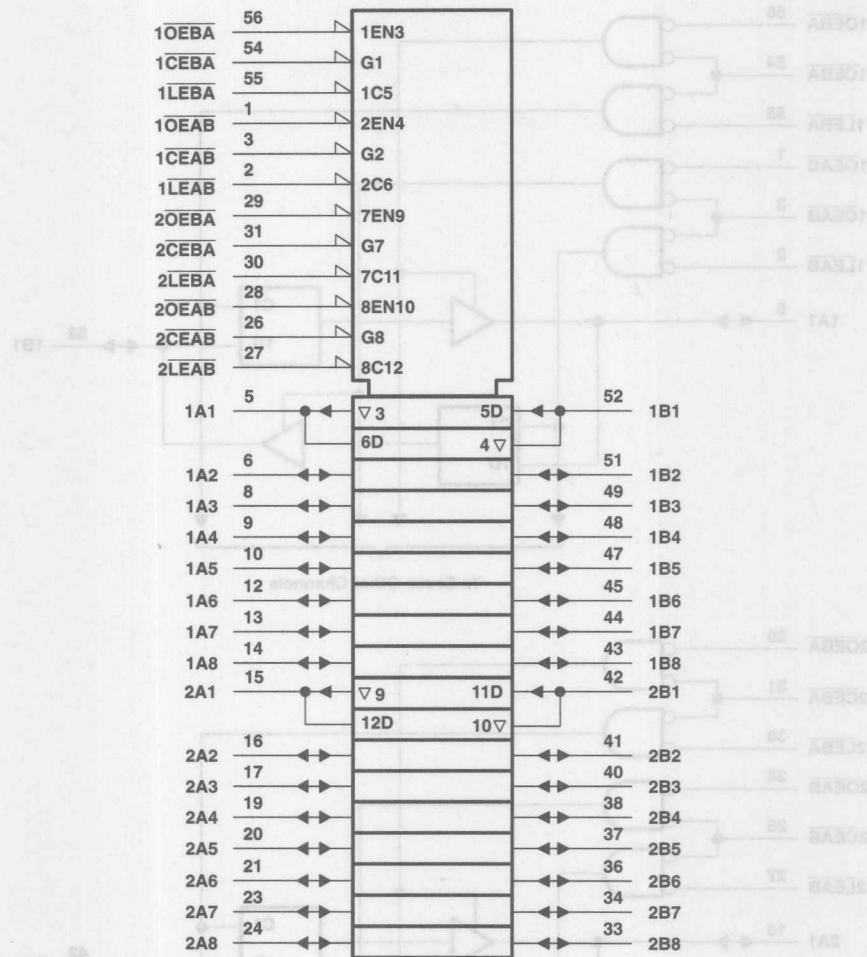
The LVTH16543 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low to enter data from A to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent, a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

SN54LVTH16543, SN74LVTH16543
3.3-V ABT 16-BIT REGISTERED TRANSCIEVERS
WITH 3-STATE OUTPUTS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

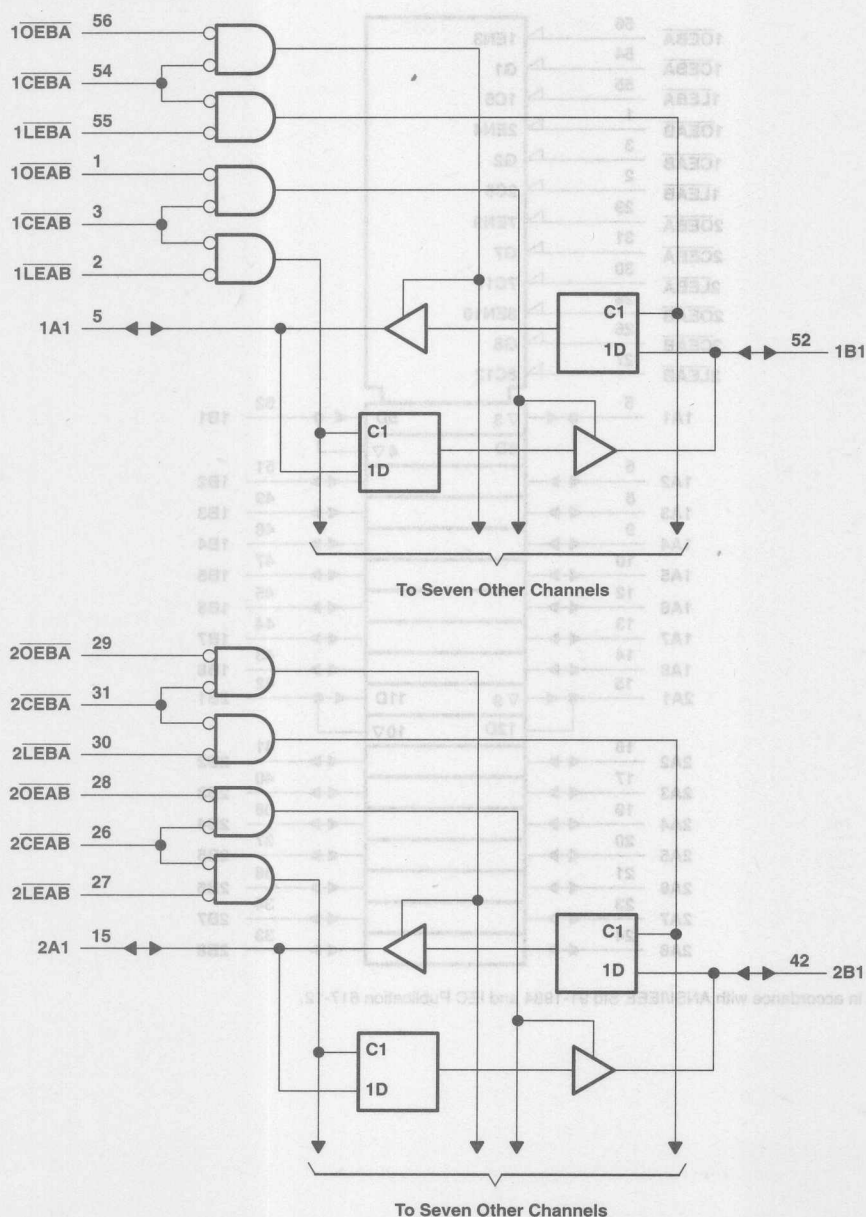


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SN54LVTH16543, SN74LVTH16543
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
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logic diagram (positive logic)



**TEXAS
INSTRUMENTS**

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SN54LVTH16543, SN74LVTH16543 **3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS** **WITH 3-STATE OUTPUTS**

SCBS699C – JULY 1997 – REVISED MARCH 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16543	96 mA
SN74LVTH16543	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16543	48 mA
SN74LVTH16543	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16543		SN74LVTH16543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVTH16543, SN74LVTH16543
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVTH16543			SN74LVTH16543			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$	2			2			
V_{OL}	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
		$I_{OL} = 24\text{ mA}$		0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$		0.4			0.4	
		$I_{OL} = 32\text{ mA}$		0.5			0.5	
		$I_{OL} = 48\text{ mA}$ $I_{OL} = 64\text{ mA}$		0.55			0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$		± 1			± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$		10			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$		20			20	
		$V_{CC} = 3.6\text{ V}$, $V_I = 0$		1 -5			1 -5	
I_{off}	$V_{CC} = 0$, V_I or $V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_I(\text{hold})$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$	75		75			μA
		$V_{CC} = 3\text{ V}$, $V_I = 2\text{ V}$	-75		-75			
I_{OZPU}	$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}	$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}	$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA
		Outputs low		5			5	
		Outputs disabled		0.19			0.19	
ΔI_{CC}^\S	$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i	$V_I = 3\text{ V or } 0$			4			4	pF
C_{io}	$V_O = 3\text{ V or } 0$			10			10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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SN54LVTH16543, SN74LVTH16543
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH16543				SN74LVTH16543				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LEAB or LEBA low		3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	A or B before LEAB↑ or LEBA↑	Data high	0.5	0.5		0.5		0.5		ns
			Data low	0.8	1.3		0.8		1.3		
		A or B before CEAB↑ or CEBA↑	Data high	0	0		0		0		ns
			Data low	0.6	1.1		0.6		1.1		
t_h	Hold time	A or B after LEAB↑ or LEBA↑	Data high	1.5	0.7		1.5		0.7		ns
			Data low	1.2	1.3		1.2		1.3		
		A or B after CEAB↑ or CEBA↑	Data high	1.7	0.9		1.7		0.9		ns
			Data low	1.6	1.8		1.6		1.8		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16543				SN74LVTH16543				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
tPLH	A or B	B or A	1.1	3.4		3.9	1.2	2.3	3.2		3.7	ns
tPHL			1.1	3.4		3.9	1.2	2.1	3.2		3.7	
tPLH	LE	A or B	1.2	4.1		5.1	1.3	2.5	3.9		4.9	ns
tPHL			1.2	4.1		5.1	1.3	2.3	3.9		4.9	
tPZH	OE	A or B	1.2	4.5		5.6	1.3	2.8	4.3		5.4	ns
tPZL			1.2	4.5		5.6	1.3	2.8	4.3		5.4	
tPHZ	OE	A or B	1.9	4.9		5.4	2	3.5	4.7		5.2	ns
tPLZ			1.9	4.6		4.7	2	3.3	4.4		4.5	
tPZH	CE	A or B	1.2	4.7		5.8	1.3	3	4.5		5.6	ns
tPZL			1.2	4.7		5.8	1.3	3	4.5		5.6	
tPHZ	CE	A or B	1.9	5.1		5.6	2	3.6	4.9		5.4	ns
tPLZ			1.9	4.9		5.1	2	3.5	4.7		4.9	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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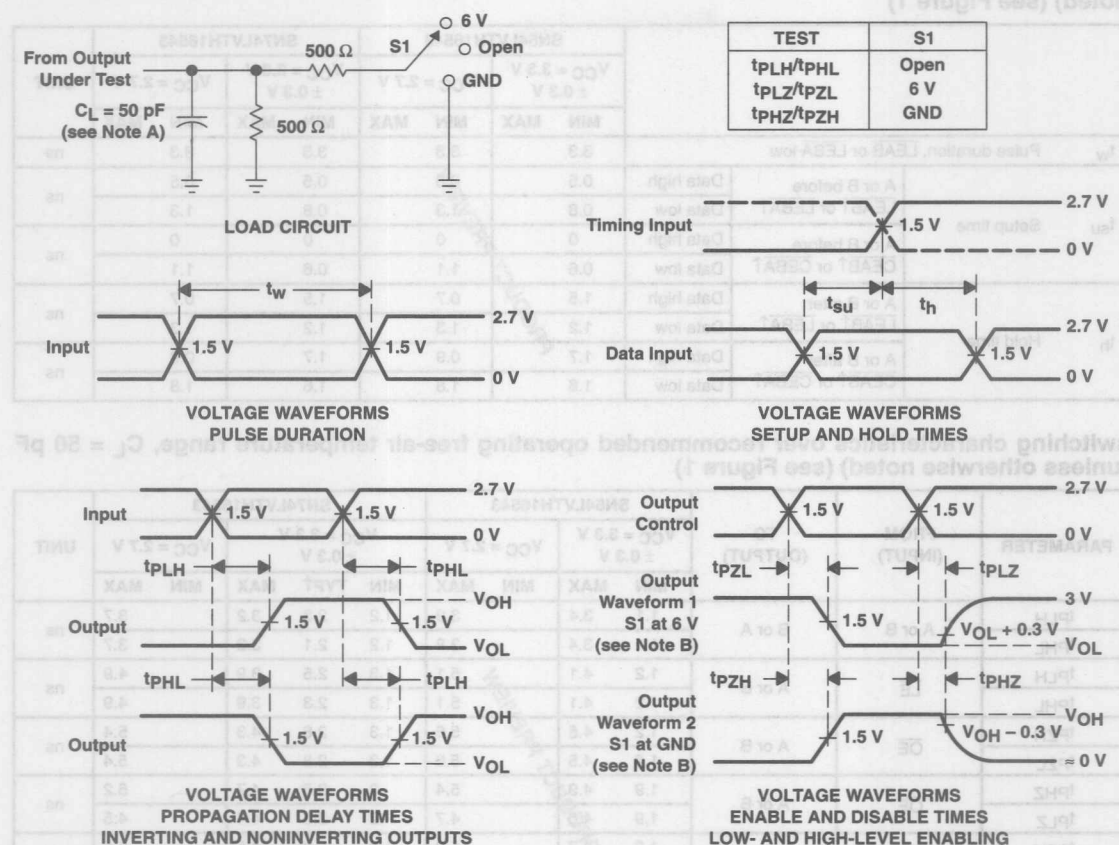
 **TEXAS
INSTRUMENTS**

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SN54LVTH16543, SN74LVTH16543 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS699C – JULY 1997 – REVISED MARCH 1998

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS698D – JULY 1997 – REVISED APRIL 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16646 . . . WD PACKAGE
SN74LVTH16646 . . . DGG OR DL PACKAGE
(TOP VIEW)

1DIR	1	56	1OE
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	2OE

description

The 'LVTH16646 devices are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16646 devices.

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SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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description (continued)

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16646 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16646 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
\overline{OE}	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
X	X	\uparrow	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	\uparrow	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	\uparrow	X	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

[†] The data-output functions may be enabled or disabled by various signals at \overline{OE} or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

SN54LVTH16646, SN74LVTH16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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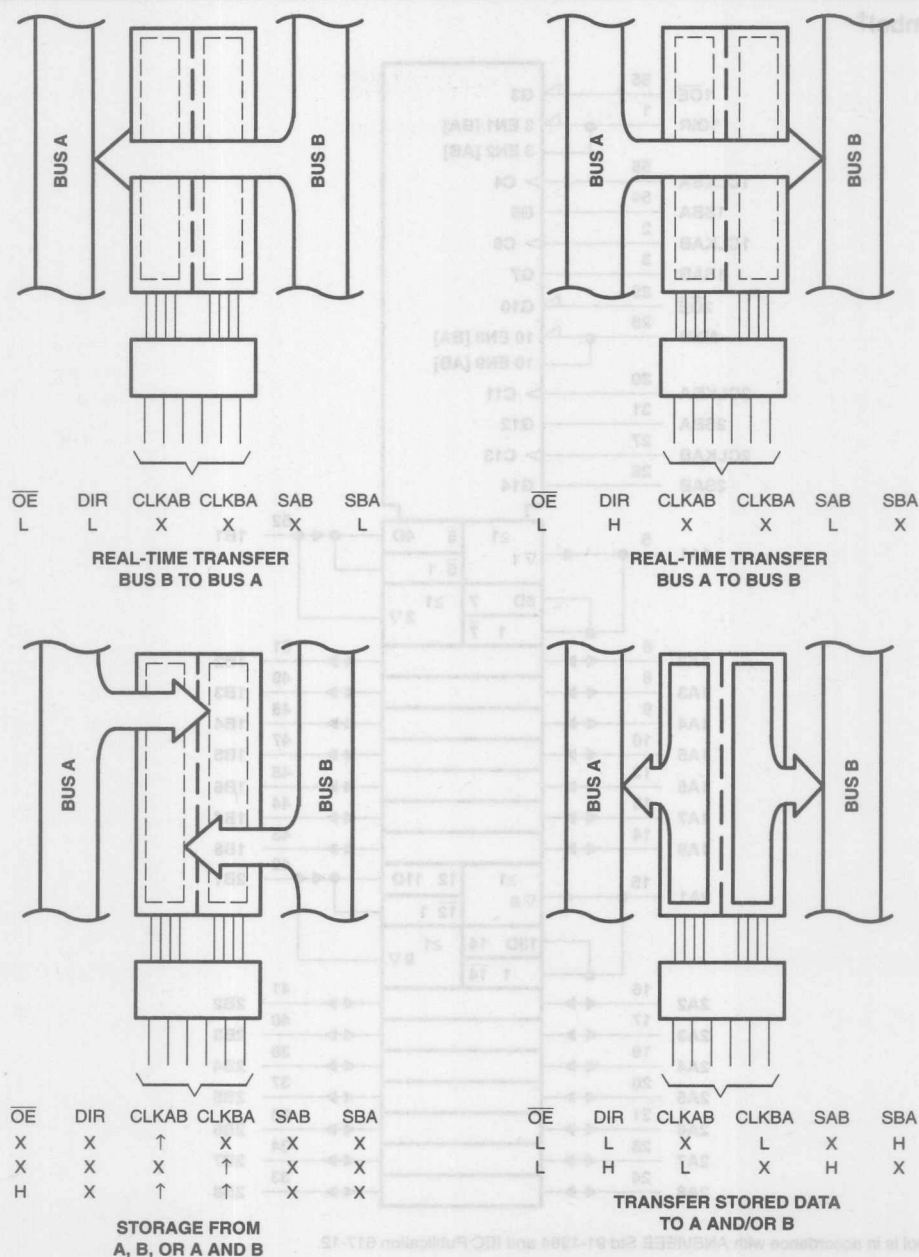
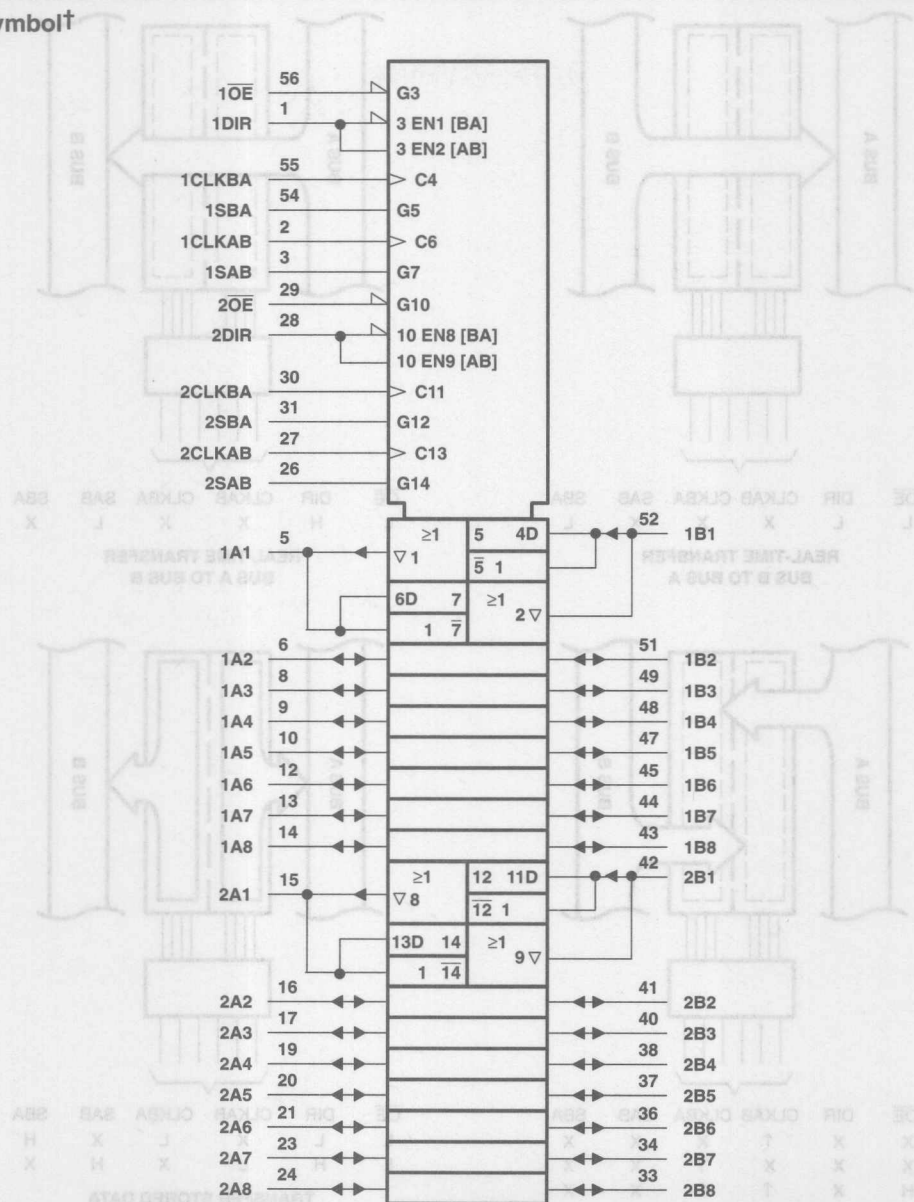


Figure 1. Bus-Management Functions

SN54LVTH16646, SN74LVTH16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

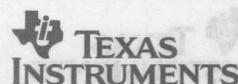
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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[illegible]

SN54LVTH16646, SN74LVTH16646 **3.3-V ABT 16-BIT BUS TRANSCEIVERS** **WITH 3-STATE OUTPUTS**

SCBS698D – JULY 1997 – REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16646	96 mA
SN74LVTH16646	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16646	48 mA
SN74LVTH16646	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

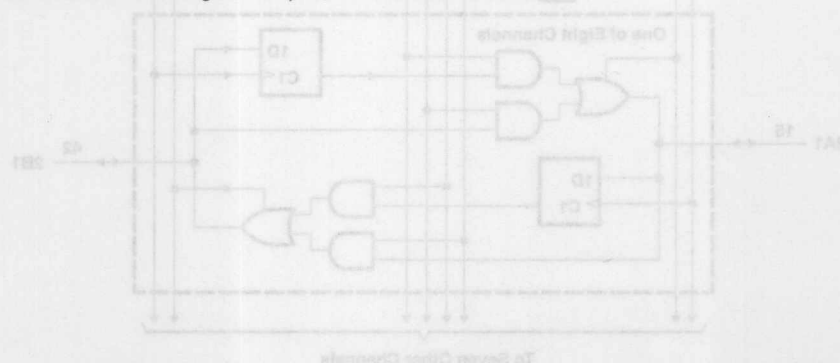
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16646		SN74LVTH16646		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16646		SN74LVTH16646		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA			-1.2		-1.2	V
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2		V	
		V _{CC} = 2.7 V, I _{OH} = -8 mA	2.4		2.4			
		V _{CC} = 3 V, I _{OH} = -24 mA	2					
		V _{CC} = 3 V, I _{OH} = -32 mA			2			
V _{OL}		V _{CC} = 2.7 V, I _{OL} = 100 μA			0.2		0.2	V
		V _{CC} = 2.7 V, I _{OL} = 24 mA			0.5		0.5	
		V _{CC} = 2.7 V, I _{OL} = 16 mA			0.4		0.4	
		V _{CC} = 3 V, I _{OL} = 32 mA			0.5		0.5	
		V _{CC} = 3 V, I _{OL} = 48 mA			0.55			
		V _{CC} = 3 V, I _{OL} = 64 mA					0.55	
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND			±1		±1	μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V			10		10	
	A or B ports‡	V _{CC} = 3.6 V, V _I = 5.5 V			20		20	
		V _{CC} = 3.6 V, V _I = V _{CC}			1		1	
		V _{CC} = 3.6 V, V _I = 0			-5		-5	
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					±100	μA
I _I (hold)	A or B ports	V _{CC} = 3 V, V _I = 0.8 V		75		75		μA
		V _{CC} = 3 V, V _I = 2 V		-75		-75		
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care			±100*		±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care			±100*		±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19		0.19	mA
			Outputs low		5		5	
			Outputs disabled		0.19		0.19	
ΔI _{CC} §		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND			0.2		0.2	mA
C _i		V _I = 3 V or 0		4		4		pF
C _{io}		V _O = 3 V or 0		10		10		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

THU	SN54LVTH16646		SN54LVTH16646				SN74LVTH16646				UNIT		
	XAM 14Y1 MIN		XAM 14Y1 MIN		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V	
	V	5.1~	V	5.1~	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX
f _{clock}	Clock frequency				150		150		150		150		MHz
t _w	Pulse duration, CLK high or low				3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑		Data high	1.2		1.5		1.2		1.5		ns	
			Data low	2		2.8		2		2.8			
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑		Data high	0.5		0		0.5		0		ns	
			Data low	0.5		0.5		0.5		0.5			

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16646				SN74LVTH16646				UNIT	
			VCC = 3.3 V ± 0.3 V		VCC = 2.7 V		VCC = 3.3 V ± 0.3 V			VCC = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
fmax			150		150		150			150		MHz
tPLH	CLKBA or CLKAB	A or B	1.3	4.5		5	1.3	2.8	4.2		4.7	ns
tPHL			1.3	4.5		5	1.3	2.8	4.2		4.7	
tPLH	A or B	B or A	1	3.6		4.1	1	2.4	3.4		3.9	ns
tPHL			1	3.6		4.1	1	2.1	3.4		3.9	
tPLH	SBA or SAB‡	A or B	1	4.7		5.6	1	2.8	4.5		5.4	ns
tPHL			1	4.7		5.6	1	3	4.5		5.4	
tPZH	OE	A or B	1	4.5		5.4	1	2.5	4.3		5.2	ns
tPZL			1	4.5		5.4	1	2.6	4.3		5.2	
tPHZ	OE	A or B	2	5.8		6.3	2	4	5.6		6.1	ns
tPLZ			2	5.6		6.3	2	3.6	5.4		6.1	
tPZH	DIR	A or B	1	4.6		5.5	1	3	4.4		5.3	ns
tPZL			1	4.6		5.5	1	3	4.4		5.3	
tPHZ	DIR	A or B	1.5	6		7.1	1.5	3.9	5.7		6.8	ns
tPLZ			1.5	5.5		6	1.5	3.6	5.2		5.7	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

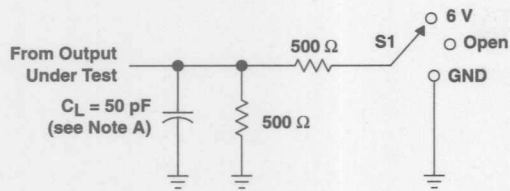


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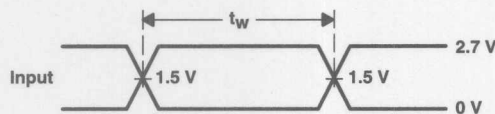
SN54LVTH16646, SN74LVTH16646
3.3-V ABT 16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS698D - JULY 1997 - REVISED APRIL 1998

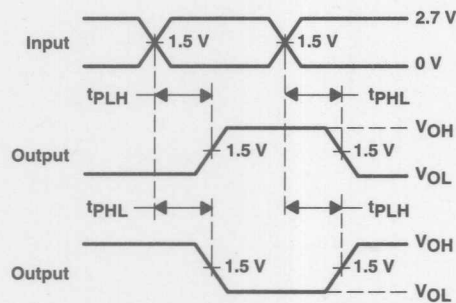
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

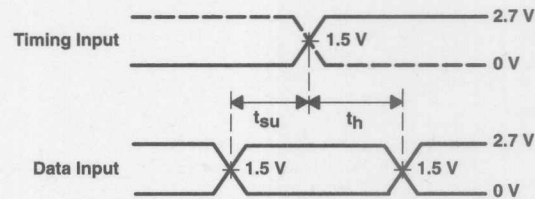


VOLTAGE WAVEFORMS
PULSE DURATION

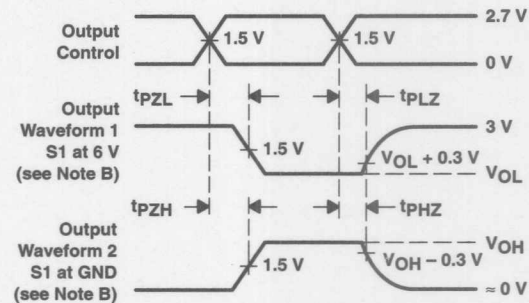


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



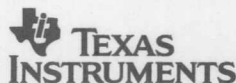
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms



SN54LVTH16652, SN74LVTH16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS150J – JULY 1994 – REVISED APRIL 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16652 ... WD PACKAGE
SN74LVTH16652 ... DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

description

The 'LVTH16652 devices are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16652 devices.

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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54LVTH16652, SN74LVTH16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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description (continued)

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54LVTH16652 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16652 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

The LVTH16652 devices are 16-bit bus transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver.

Output-enable (OEAB and OEBA) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the LVTH16652 devices.

SN54LVTH16652, SN74LVTH16652
3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

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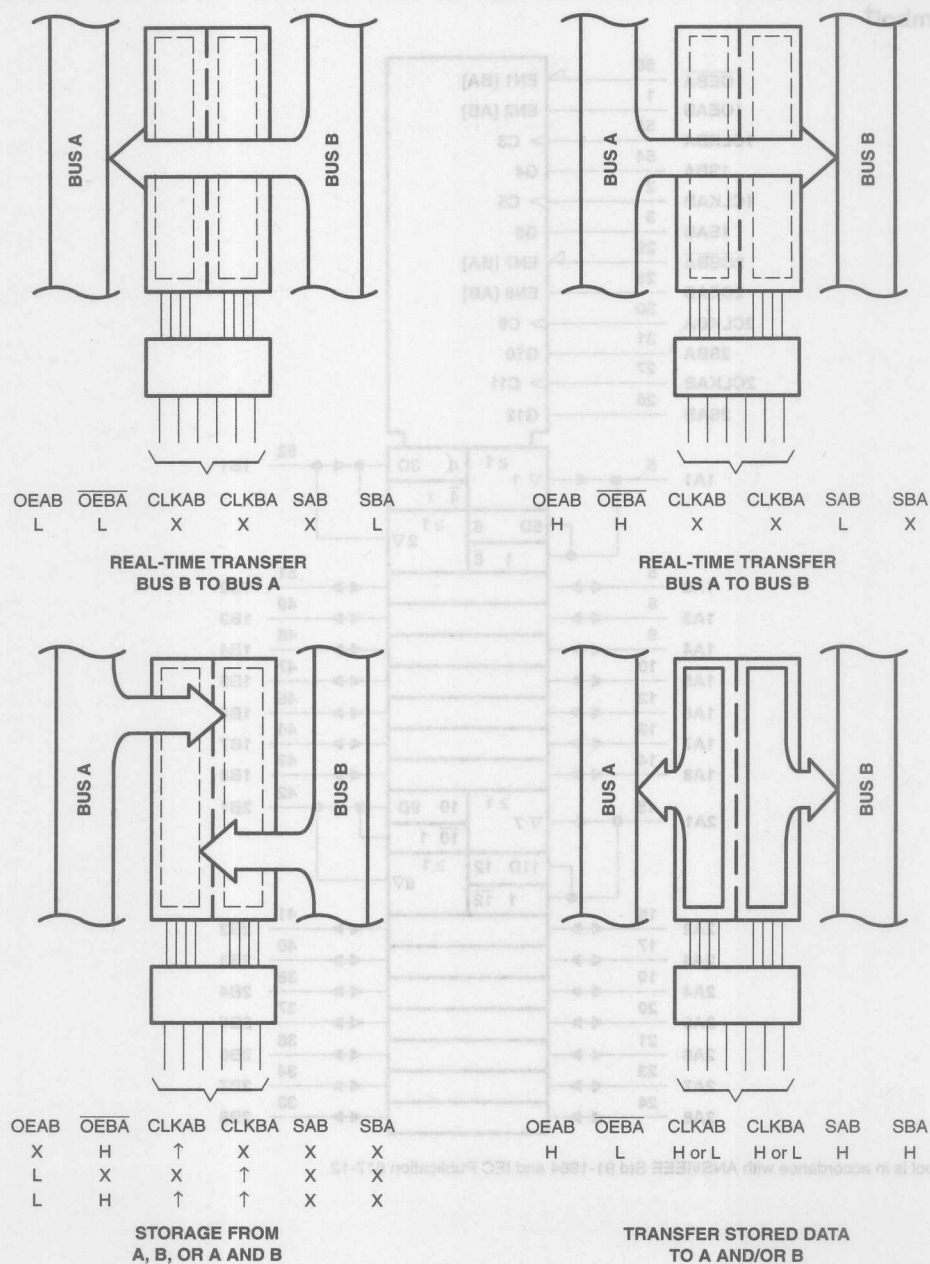


Figure 1. Bus-Management Functions

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The diagram shows the pinout of the 68000 microprocessor. The pins are numbered 1 through 56. The connections are as follows:

- 1OEBA: 56
- 1OEAB: 1
- 1CLKBA: 55
- 1SBA: 54
- 1CLKAB: 2
- 1SAB: 3
- 2OEBA: 29
- 2OEAB: 28
- 2CLKBA: 30
- 2SBA: 31
- 2CLKAB: 27
- 2SAB: 26
- EN1 [BA]: 56
- EN2 [AB]: 1
- C3: 55
- G4: 54
- C5: 2
- G6: 3
- EN7 [BA]: 29
- EN8 [AB]: 28
- C9: 30
- G10: 31
- C11: 27
- G12: 26
- 1A1: 5
- 1A2: 6
- 1A3: 8
- 1A4: 9
- 1A5: 10
- 1A6: 12
- 1A7: 13
- 1A8: 14
- 2A1: 15
- 2A2: 16
- 2A3: 17
- 2A4: 19
- 2A5: 20
- 2A6: 21
- 2A7: 23
- 2A8: 24
- 1B1: 52
- 1B2: 51
- 1B3: 49
- 1B4: 48
- 1B5: 47
- 1B6: 45
- 1B7: 44
- 1B8: 43
- 2B1: 42
- 2B2: 41
- 2B3: 40
- 2B4: 38
- 2B5: 37
- 2B6: 36
- 2B7: 34
- 2B8: 33

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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SN54LVTH16652, SN74LVTH16652 **3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS** **WITH 3-STATE OUTPUTS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16652	96 mA
SN74LVTH16652	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16652	48 mA
SN74LVTH16652	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

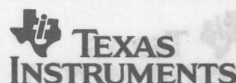
- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16652		SN74LVTH16652		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54LVTH16652, SN74LVTH16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16652		SN74LVTH16652		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V,	I _I = -18 mA			-1.2		V
V _{OH}		V _{CC} = 2.7 V to 3.6 V,	I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		V _{CC} = 2.7 V,	I _{OH} = -8 mA	2.4		2.4		
		V _{CC} = 3 V	I _{OH} = -24 mA	2		2		
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA			0.2		V
			I _{OL} = 24 mA			0.5		
		V _{CC} = 3 V	I _{OL} = 16 mA			0.4		
			I _{OL} = 32 mA			0.5		
			I _{OL} = 48 mA			0.55		
			I _{OL} = 64 mA			0.55		
I _I	Control inputs	V _{CC} = 0 or 3.6 V,	V _I = 5.5 V	10		10		μA
		V _{CC} = 3.6 V,	V _I = V _{CC} or GND	±1		±1		
	A or B ports‡	V _{CC} = 3.6 V	V _I = 5.5 V	20		20		
		V _{CC} = 3.6 V	V _I = V _{CC}	1		1		
			V _I = 0	-5		-5		
I _{off}		V _{CC} = 0,	V _I or V _O = 0 to 4.5 V			±100		μA
I _I (hold)	A or B ports	V _{CC} = 3 V	V _I = 0.8 V	75		75		μA
			V _I = 2 V	-75		-75		
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE/OE = don't care		±100*		±100		μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	0.19		0.19		mA
			Outputs low	5		5		
			Outputs disabled	0.19		0.19		
ΔI _{CC} §		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA
C _i		V _I = 3 V or 0		4		4		pF
C _{io}		V _O = 3 V or 0		10		10		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.

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SN54LVTH16652, SN74LVTH16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS150J – JULY 1994 – REVISED APRIL 1998

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

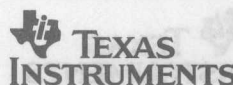
TMU	S289THVTH16652		S289THVTH16652		SN54LVTH16652				SN74LVTH16652				UNIT
	XAM 14VVT MIN		XAM 14VVT MIN		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
	V	S.1-	S.1-		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency				150		150		150		150		MHz
t _w	Pulse duration, CLK high or low				3.3		3.3		3.3		3.3		ns
t _{su}	Setup time, A or B before CLKAB↑ or CLKBA↑		Data high	1.2		1.5		1.2		1.5		ns	
			Data low	2		2.8		2		2.8			
t _h	Hold time, A or B after CLKAB↑ or CLKBA↑		Data high	0.5		0		0.5		0		ns	
			Data low	0.5		0.5		0.5		0.5			

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16652				SN74LVTH16652				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f _{max}			150		150		150			150		MHz
t _{PLH}	CLK	B or A	1.3	4.5		5	1.3	2.7	4.2		4.7	ns
t _{PHL}			1.3	4.5		5	1.3	2.8	4.2		4.7	
t _{PLH}	A or B	B or A	1	3.6		4.1	1	2.4	3.4		3.9	ns
t _{PHL}			1	3.6		4.1	1	2.1	3.4		3.9	
t _{PLH}	SAB or SBA	B or A	1	4.7		5.6	1	2.7	4.5		5.4	ns
t _{PHL}			1	4.7		5.6	1	3	4.5		5.4	
t _{PZH}	OEBA	A	1	4.5		5.4	1	2.4	4.3		5.2	ns
t _{PZL}			1	4.5		5.4	1	2.3	4.3		5.2	
t _{PHZ}	OEBA	A	2	5.8		6.3	2	3.9	5.6		6.1	ns
t _{PLZ}			2	5.6		6.3	2	3.4	5.4		6.1	
t _{PZH}	OEAB	B	1.3	4.4		5.1	1.3	2.7	4.2		4.9	ns
t _{PZL}			1.3	4.4		5.1	1.3	2.6	4.2		4.9	
t _{PHZ}	OEAB	B	1.6	5.8		6.5	1.3	3.5	5.5		6.2	ns
t _{PLZ}			1.6	5.8		6.5	1.3	3.2	5.5		6.2	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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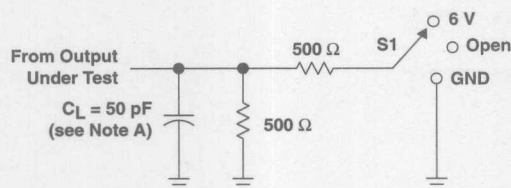


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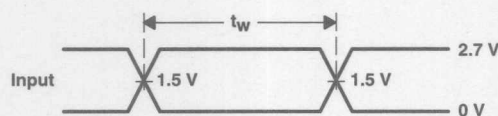
SN54LVTH16652, SN74LVTH16652 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS150J – JULY 1994 – REVISED APRIL 1998

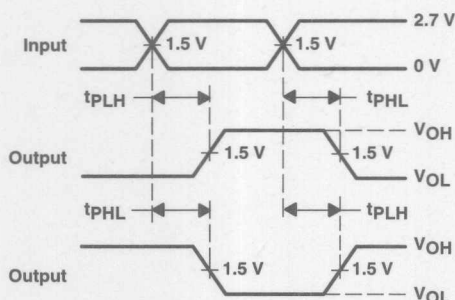
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

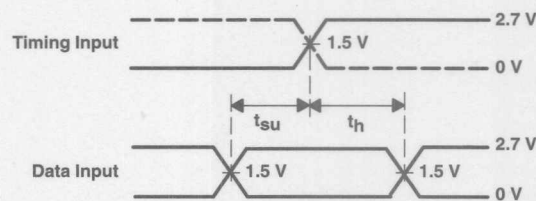


VOLTAGE WAVEFORMS
PULSE DURATION

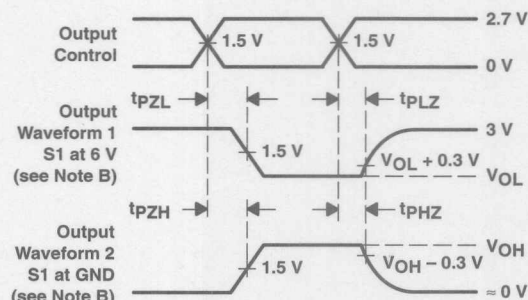


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

SCBS713A – MARCH 1998 – REVISED MARCH 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16835 ... WD PACKAGE
SN74LVTH16835 ... DGG OR DL PACKAGE
(TOP VIEW)

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
V_{CC}	7	50	V_{CC}
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
V_{CC}	22	35	V_{CC}
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
\overline{OE}	27	30	CLK
LE	28	29	GND

NC – No internal connection

description

The 'LVTH16835 devices are 18-bit universal bus drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. These devices operate in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of the clock. When \overline{OE} is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PRODUCT PREVIEW

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**TEXAS
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SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

SCBS713A – MARCH 1998 – REVISED MARCH 1998

description (continued)

The SN54LVTH16835 is characterized for operation over the full military temperature range of -55°C to 125°C .
The SN74LVTH16835 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	\uparrow	L	L
L	L	\uparrow	H	H
L	L	H	X	Y_0^{\dagger}
L	L	L	X	Y_0^{\ddagger}

\dagger Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

\ddagger Output level before the indicated steady-state input conditions were established

PRODUCT PREVIEW

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Data flow from A to Y is controlled by the output-enable (OE) input. These devices operate in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch flip-flop on the low-to-high transition of the clock. When OE is high, the outputs are in the high-impedance state.

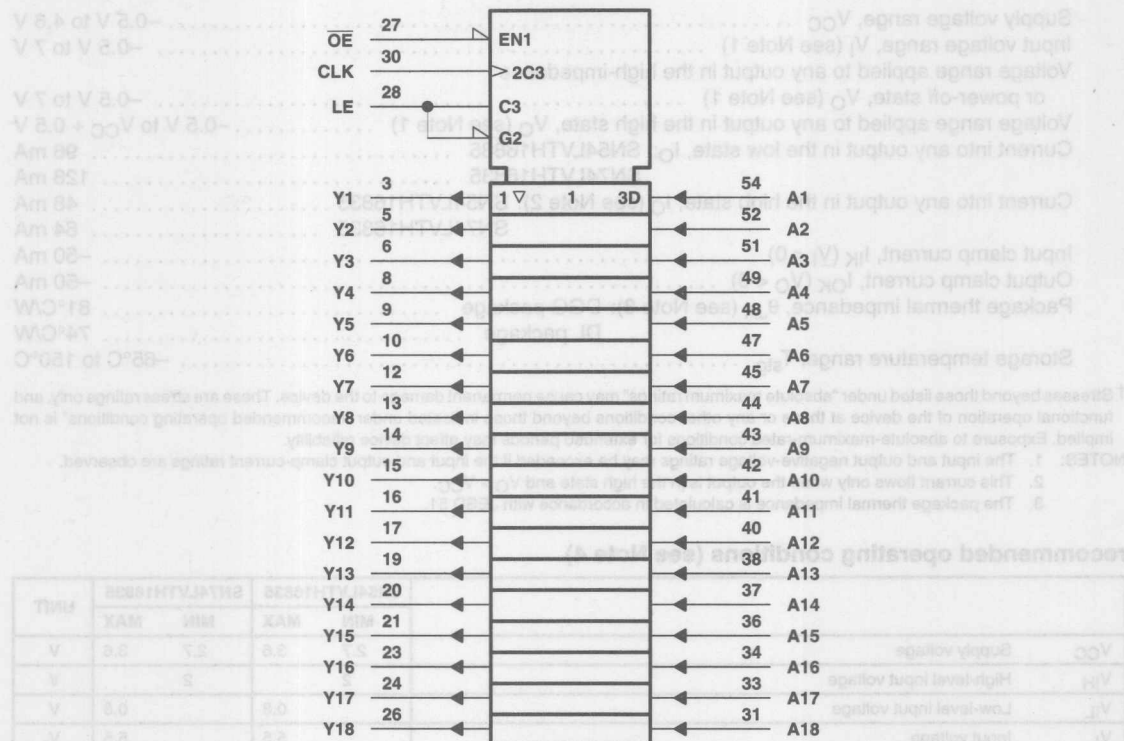
The LVTH16835 devices are 18-bit universal bus drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.



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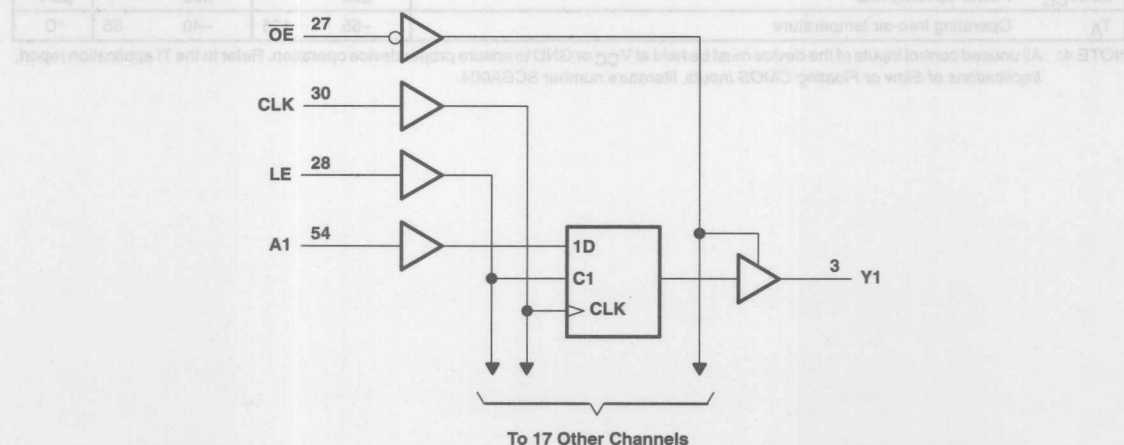
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCT PREVIEW

SN54LVTH16835, SN74LVTH16835 **3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS** **WITH 3-STATE OUTPUTS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16835	96 mA
SN74LVTH16835	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16835	48 mA
SN74LVTH16835	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

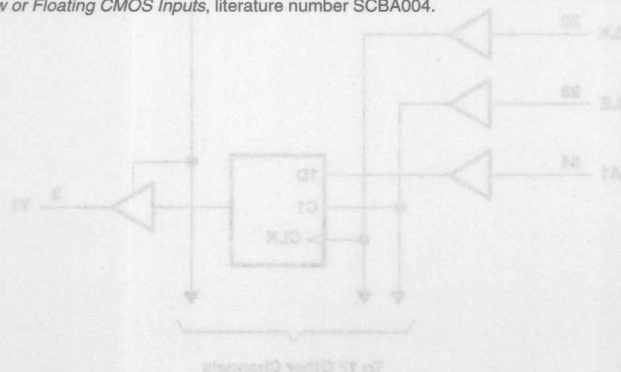
- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16835		SN74LVTH16835		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

PRODUCT PREVIEW



**TEXAS
INSTRUMENTS**

SN54LVTH16835, SN74LVTH16835
3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16835		SN74LVTH16835		UNIT
			MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA			-1.2	-1.2	V
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA	V _{CC} -0.2		V _{CC} -0.2		V
		V _{CC} = 2.7 V, I _{OH} = -8 mA	2.4		2.4		
		V _{CC} = 3 V, I _{OH} = -24 mA	2				
		V _{CC} = 3 V, I _{OH} = -32 mA			2		
V _{OL}		V _{CC} = 2.7 V	I _{OL} = 100 μA		0.2	0.2	V
			I _{OL} = 24 mA		0.5	0.5	
		V _{CC} = 3 V	I _{OL} = 16 mA		0.4	0.4	
			I _{OL} = 32 mA		0.5	0.5	
			I _{OL} = 48 mA		0.55		
			I _{OL} = 64 mA			0.55	
I _I	Control inputs	V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10	10	μA	
		V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1	±1		
	A inputs	V _{CC} = 3.6 V, V _I = V _{CC}		1	1		
		V _{CC} = 3.6 V, V _I = 5.5 V		20	20		
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100	μA
I _I (hold)	A inputs	V _{CC} = 3 V	V _I = 0.8 V	75	75		μA
			V _I = 2 V	-75	-75		
I _{OZH}		V _{CC} = 3.6 V, V _O = 3 V		1	1		μA
I _{OZL}		V _{CC} = 3.6 V, V _O = 0.5 V		-1	-1		μA
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*		±100	μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*		±100	μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		0.19	0.19	mA
			Outputs low		5	5	
			Outputs disabled		0.19	0.19	
ΔI _{CC} ‡		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2	0.2		mA
C _i	Control inputs	V _I = 3 V or 0		3.5	3.5		pF
	Data inputs			4.5	4.5		
C _O		V _O = 3 V or 0		11	11		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW



SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

UNIT	SN54LVTH16835		SN74LVTH16835		SN54LVTH16835				SN74LVTH16835				UNIT
					V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		150		150		150		150		MHz		
t _w	Pulse duration	LE high		3.3		3.3		3.3		3.3		ns	
		CLK high or low		3.3		3.3		3.3					
t _{su}	Setup time	Data before CLK↑		1.6		2.1		1.6		2.1		ns	
		Data before LE↓	CLK high	2.6		1.9		2.6		1.9			
			CLK low	2		1.3		2		1.3			
t _h	Hold time	Data after CLK↑		2		2.1		2		2.1		ns	
		Data after LE↓		0.9		1.2		0.9		1.2			

switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16835				SN74LVTH16835				UNIT	
			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 2.7 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f_{max}			150		150		150		150		MHz	
t_{PLH}	A	Y	1.7	5.4	6.8		1.7	3	5.4	6.8		ns
t_{PHL}			1.6	5.9	7.7		1.6	3.2	5.9	7.7		
t_{PLH}	LE	Y	2.3	7	8.5		2.3	4	7	8.5		ns
t_{PHL}			2.7	7.9	9.7		2.7	4.3	7.9	9.7		
t_{PLH}	CLK	Y	2.5	7.9	9.2		2.5	4.1	7.9	9.2		ns
t_{PHL}			3.5	8.9	10.4		3.5	5.4	8.9	10.4		
t_{PZH}	$\overline{\text{OE}}$	Y	1.2	5	5.9		1.2	3	5	5.9		ns
t_{PZL}			1.5	5.8	6.9		1.5	3	5.8	6.9		
t_{PHZ}	$\overline{\text{OE}}$	Y	2.7	7.4	8.3		2.7	4.6	7.4	8.3		ns
t_{PLZ}			2.8	6.7	7.2		2.8	4.7	6.7	7.2		
$t_{\text{sk(o)}}^{\ddagger}$									0.5		ns	

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Skew between any two outputs of the same package switching in the same direction

PRODUCT PREVIEW

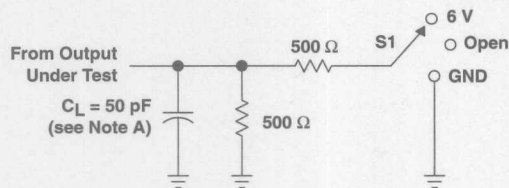


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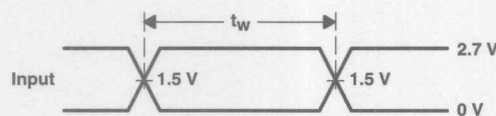
SN54LVTH16835, SN74LVTH16835
3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS
WITH 3-STATE OUTPUTS

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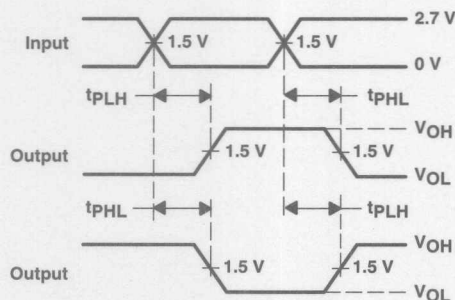
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

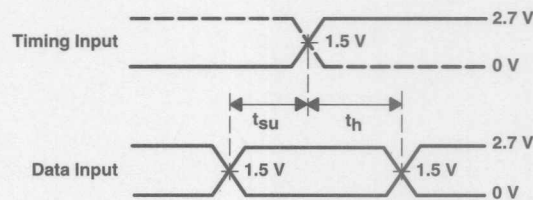


VOLTAGE WAVEFORMS
PULSE DURATION

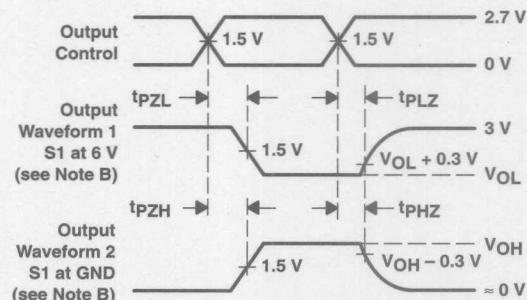


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

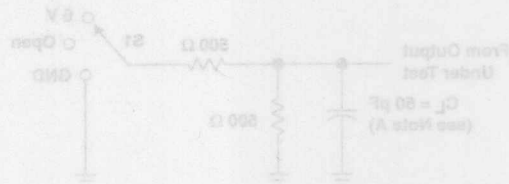
Figure 1. Load Circuit and Voltage Waveforms

PRODUCT PREVIEW

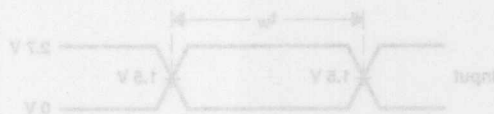


PARAMETER MEASUREMENT INFORMATION

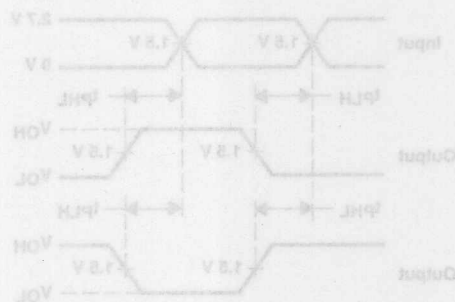
TEST	BI
Output	Open
Input	0 V
Output	GND



LOAD CIRCUIT



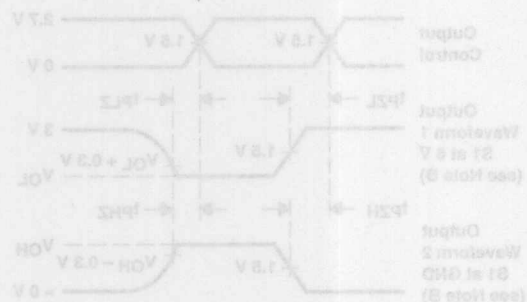
VOLTAGE WAVEFORMS
PULSE BURST



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- Includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 - Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns.
 - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

SN54LVTH16952, SN74LVTH16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH16952 ... WD PACKAGE
SN74LVTH16952 ... DGG OR DL PACKAGE
(TOP VIEW)

1OEAB	1	56	1OEBA
1CLKAB	2	55	1CLKBA
1CLKENAB	3	54	1CLKENBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2CLKENAB	26	31	2CLKENBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2OEBA

description

The 'LVTH16952 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Widebus is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LVTH16952, SN74LVTH16952

3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

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description (continued)

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16952 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH16952 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT B
CLKENAB	CLKAB	\overline{OEAB}	A	
H	X	L	X	B_0^{\ddagger}
X	L	L	X	B_0^{\ddagger}
L	\uparrow	L	L	L
L	\uparrow	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar, but uses CLKENBA , CLKBA , and \overline{OEBA} .

‡ Level of B before the indicated steady-state input conditions were established

The LVTH16952 devices are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input provided that the clock-enable (CLKENAB or CLKENBA) input is low. Taking the output-enable (\overline{OEAB} or \overline{OEBA}) input low accesses the data on either port. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

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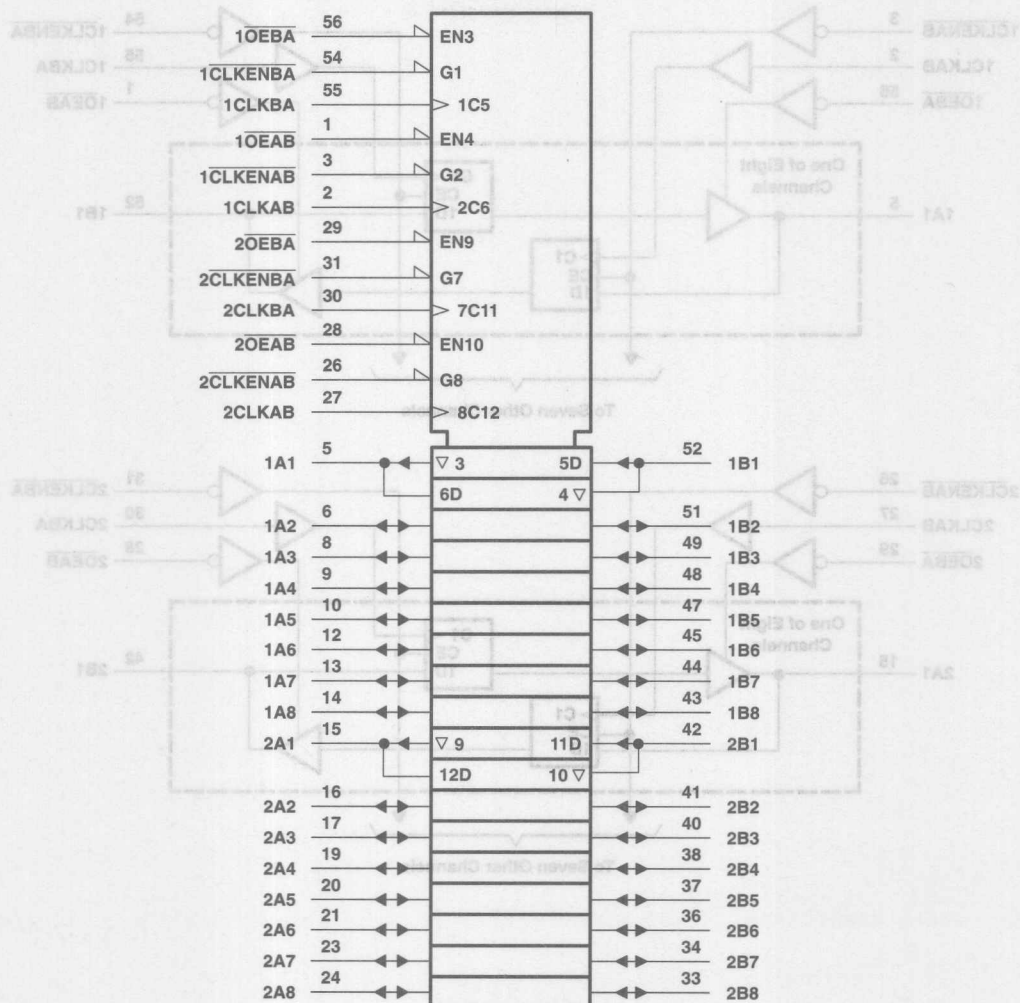


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SN54LVTH16952, SN74LVTH16952
3.3-V ABT 16-BIT REGISTERED TRANSCIEVERS
WITH 3-STATE OUTPUTS

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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

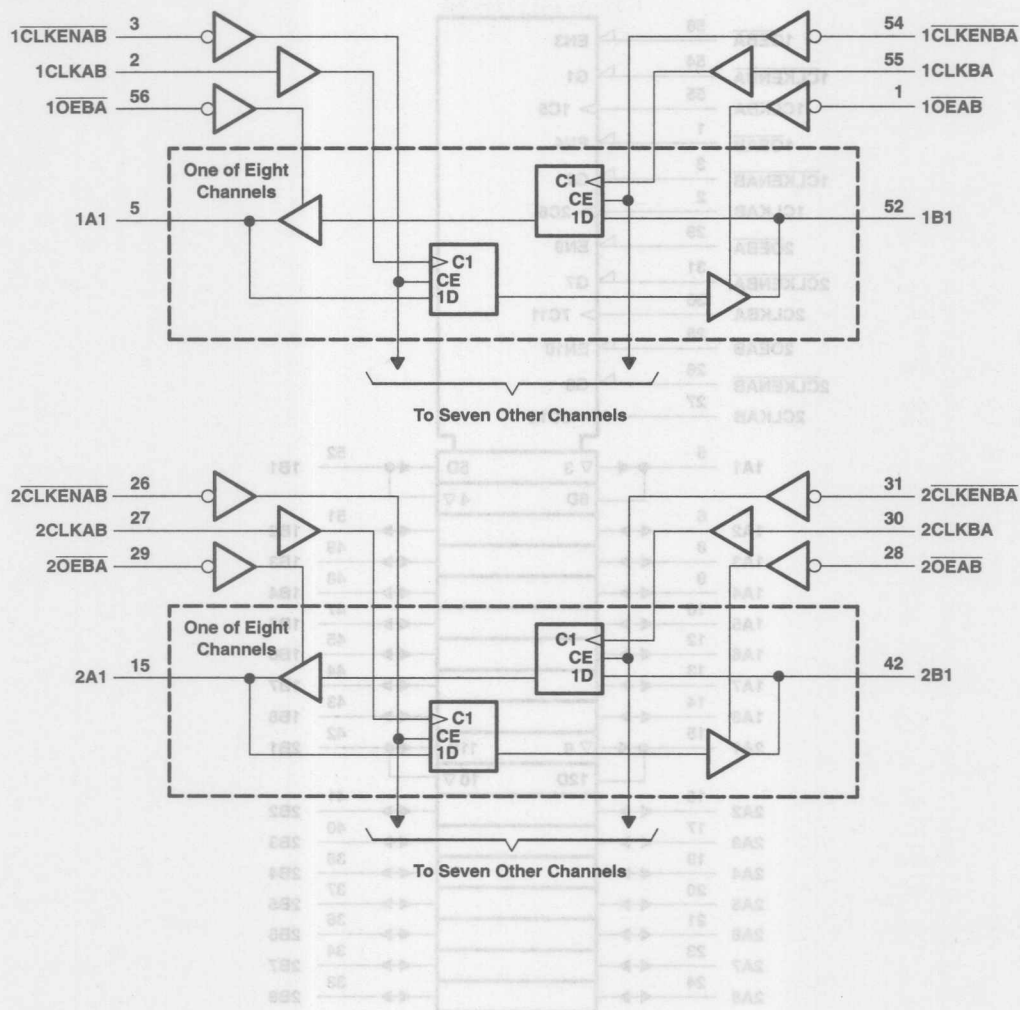


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SN54LVTH16952, SN74LVTH16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



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SN54LVTH16952, SN74LVTH16952 **3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS** **WITH 3-STATE OUTPUTS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH16952	96 mA
SN74LVTH16952	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH16952	48 mA
SN74LVTH16952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

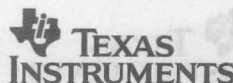
[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH16952		SN74LVTH16952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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SN54LVTH16952, SN74LVTH16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH16952			SN74LVTH16952			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$, $I_{OH} = -8\text{ mA}$	2.4			2.4			
		$V_{CC} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$ $I_{OH} = -32\text{ mA}$	2			2			
V_{OL}		$V_{CC} = 2.7\text{ V}$			0.2			0.2	V
					0.5			0.5	
					0.4			0.4	
		$V_{CC} = 3\text{ V}$			0.5			0.5	
					0.55			0.55	
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1			± 1	μA
		$V_{CC} = 0\text{ or } 3.6\text{ V}$, $V_I = 5.5\text{ V}$			10			10	
	A or B ports‡	$V_{CC} = 3.6\text{ V}$, $V_I = 5.5\text{ V}$			20			20	
		$V_I = V_{CC}$ $V_I = 0$			1 -5			1 -5	
I_{off}		$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$						± 100	μA
$I_{I(hold)}$	A or B ports	$V_{CC} = 3\text{ V}$, $V_I = 0.8\text{ V}$		75			75		μA
		$V_I = 2\text{ V}$		-75			-75		
I_{OZPU}		$V_{CC} = 0\text{ to } 1.5\text{ V}$, $V_O = 0.5\text{ V to } 3\text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{OZPD}		$V_{CC} = 1.5\text{ V to } 0$, $V_O = 0.5\text{ V to } 3\text{ V}$, OE = don't care			$\pm 100^*$			± 100	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$			0.19			0.19	mA
		Outputs high			5			5	
		Outputs disabled			0.19			0.19	
ΔI_{CC}^{\S}		$V_{CC} = 3\text{ V to } 3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
C_i		$V_I = 3\text{ V or } 0$		4			4		pF
C_{io}		$V_O = 3\text{ V or } 0$		10			10		pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused pins at $V_{CC}\text{ or GND}$

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}\text{ or GND}$.



SN54LVTH16952, SN74LVTH16952
3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH16952				SN74LVTH16952				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		150		150		150		150		MHz
t_w	Pulse duration		CLK high or low		3.3		3.3		3.3		ns
t_{su}	Setup time		A or B before CLK		1.9		2.5		1.7		2.5
			CLKEN before CLK		2		2.8		2		2.8
t_h	Hold time		A or B after CLK		0.8		0.7		0.8		0
			CLKEN after CLK		0.4		0.4		0.4		0

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

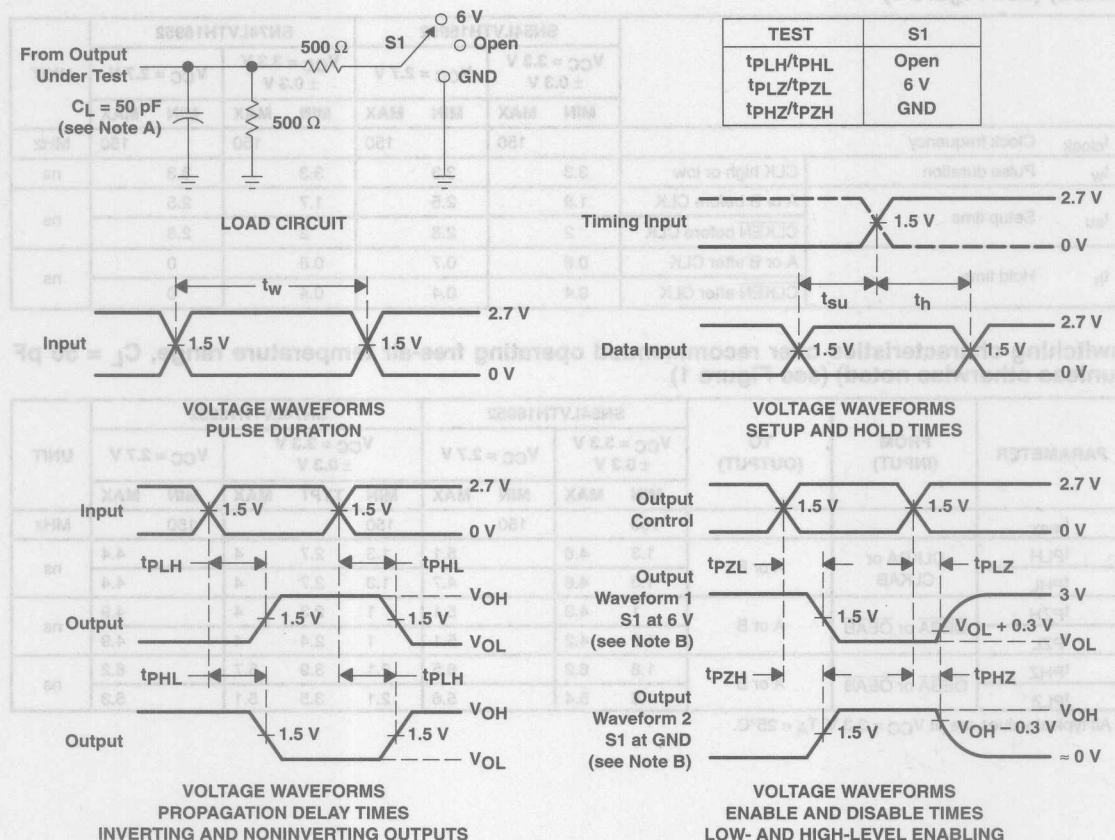
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16952				SN74LVTH16952				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f_{max}			150		150		150		150		MHz
t_{PLH}	CLKBA or CLKAB	A or B	1.3	4.6	5.1		1.3	2.7	4	4.4	ns
t_{PHL}			1.3	4.6	4.7		1.3	2.7	4	4.4	
t_{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1	4.3	5.1		1	2.3	4	4.9	ns
t_{PZL}			1.2	4.2	5.1		1	2.4	4	4.9	
t_{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1.8	6.2	6.5		2.1	3.9	5.7	6.2	ns
t_{PLZ}			1.6	5.4	5.6		2.1	3.5	5.1	5.3	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

SN54LVTH16952, SN74LVTH16952 3.3-V ABT 16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

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June 1994

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Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

- Split-rail or dual 3.3-V and 5-V V_{CC} devices
- Completely 5-V tolerant, pure 3.3-V V_{CC} components

This application report deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and datapath voltage translators, but the following precautions are usually recommended:

- Dual- V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to the devices in the event that one V_{CC} rail ramps faster than the other. These stringent requirements are often difficult to meet from a system-timing standpoint and offer little flexibility for partial system power down or other advanced power-saving design techniques.
- Simply because the device has a 5-V V_{CC} pin does not necessarily ensure that the part will actually switch all the way to the 5-V rail. Switching to 5 V is one way to reduce the power consumption in 5-V memories or other pure 5-V CMOS circuits that are driven by a level-shifter device (this application report will demonstrate others as well).

The data sheet for the product in question reveals whether the part drives all the way to the 5-V rail. If the output high-voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs typically drive only to around 3.6 V.

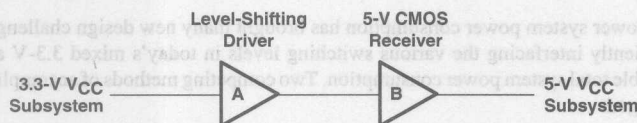
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices previously mentioned. From a single V_{CC} source, they avoid the power-sequencing problems of the split rails and also are offered in a number of functions, bit widths, and storage options. The one potential drawback of the single- V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail. But, is this really a drawback?

The Misconception About ΔI_{CC}

The component selection of a level shifter impacts two major aspects of total system-power dissipation:

- The impact that the V_{OH} level of the driving part (A, in Figure 1) has on the power dissipation of the receiving device (B, in Figure 1), commonly known as ΔI_{CC}
- The power of the device itself



Note: Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B, in Figure 1) due to the V_{OH} level of the driving device (A, in Figure 1). It would be correct to expect that a TTL-compatible 5-V CMOS product have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from 0 to V_{CC} .

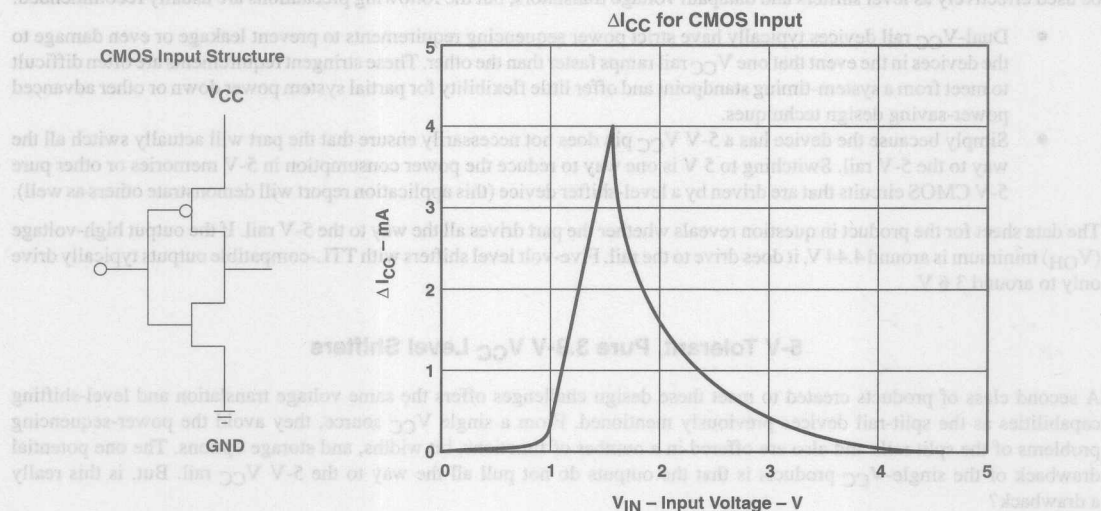


Figure 2. Basic CMOS Input Structure and Typical ΔI_{CC} Current

As expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V.

Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

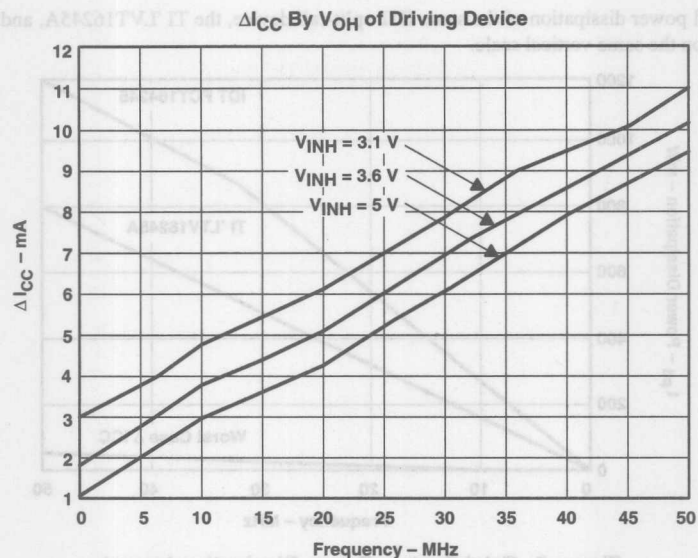


Figure 3. ΔI_{CC} - 16-Bit Device

As shown in Figure 3, ΔI_{CC} is, in fact, 2 to 3 mA higher for the case where V_{OH} is only 3.1 V, than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the impact of system power on the driving device.

Figure 4 shows the V_{OH} of two devices: the FCT164245 split-rail device from Integrated Device Technologies (IDT) and the 'LVT16245A from Texas Instruments.

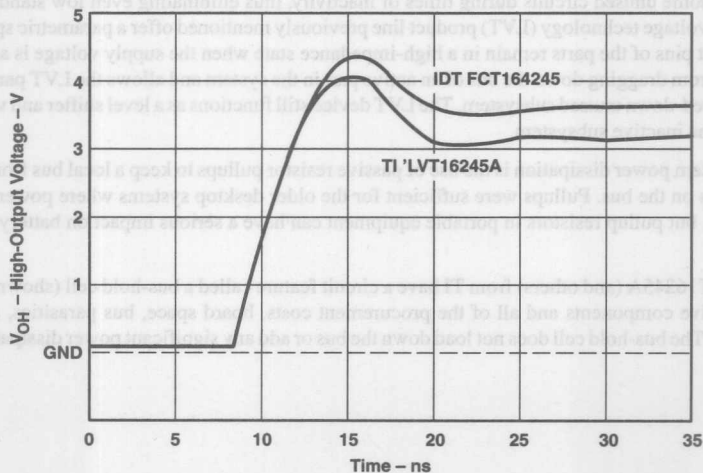


Figure 4. V_{OH} of FCT164245 and 'LVT16245A

From Figure 4, it can be correctly concluded that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total system power dissipation that selection of a level-shifter device has from a system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI 'LVT16245A, and the worst-case ΔI_{CC} ($V_{OH} = 3.1$ V) plotted on the same vertical scale.

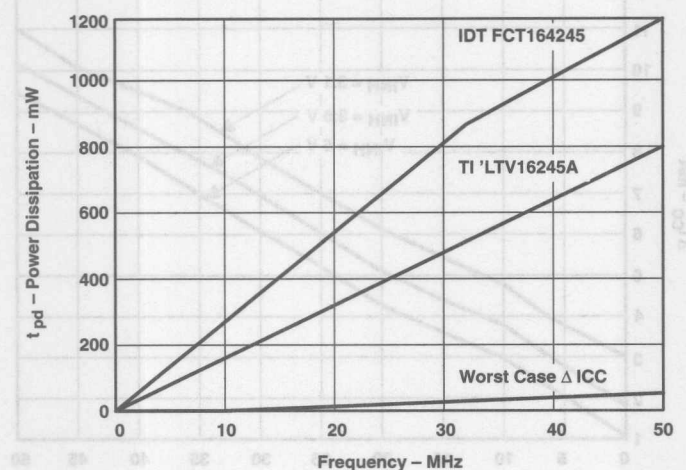


Figure 5. Total-System Power-Dissipation Impact

From Figure 5, it can be seen that, even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} is more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's low-voltage technology (LVT) product line previously mentioned offer a parametric specification I_{off} , which ensures that the output pins of the parts remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT device from dragging down the bus of an active part in the system and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating and causing damage to the devices on the bus. Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the 'LVT16245A (and others) from TI have a circuit feature called a bus-hold cell (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

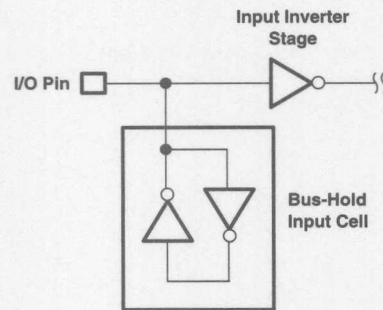


Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by the judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Acknowledgment

The author of this document is Mark McClear.

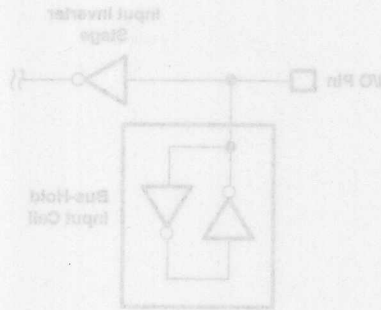


Figure 6. 1VT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by the judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect the voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Acknowledgment

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Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices

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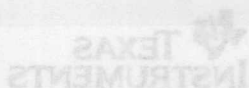
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Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices

Users of Texas Instruments (TI™) SLL products must consider device power dissipation, package power capability, and maximum ambient temperatures when designing with these products. The product users also need to be aware of the long-term reliability impact of maximum device-junction temperatures.

This application report is intended to help users understand and evaluate these factors. Three concepts — package thermal performance, device power dissipation, and reliability — are discussed in separate sections.

The first section, *Package Thermal Performance*, includes data about the recently developed EIA/JEDEC Standard JESD 51 for package thermal-impedance measurement. It discusses most SLL package types and lists θ_{JA} (thermal impedance) values for those packages.

The second section, *Power Calculation*, discusses the power consumption by CMOS and BiCMOS/bipolar semiconductors. Standard formulas are given that allow the user to calculate the maximum power dissipated by a device in a typical application using data-book specifications, operating frequency, and voltage. The only characteristic not readily known is the output loading of the devices under consideration.

The third section, *Benefits of Minimizing Power Consumption*, discusses ways to reduce power consumption and the benefits thereof.

The final section, *Reliability Implications*, discusses the effects of chip temperature on reliability and electromigration. Information presented in this section allows the user to make an informed judgment as to the maximum chip temperature versus device wearout acceptable in the particular application.

The recommended analysis procedure is to assume a maximum chip temperature (see *Reliability Implications*) then, using θ_{JA} values for the chosen package (see *Package Thermal Performance*) and the known environmental requirements, calculate the maximum permissible power for that package. The formula presented in the *Power Calculation* section can then be used to ensure the operating conditions do not exceed the power capability of the chosen package type. Of course, the user can choose to calculate the maximum power from the application, then select a package that can meet the power dissipation requirement.

Key features of the standard test-board design are:

- Board thickness: 0.082 in.
- Board dimensions: 4.0 x 4.2 in. (for packages > than 27 mm in length)
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to JEDEC 51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermalCAL, a finite-difference thermal-modeling tool.

Given SLL packages were tested using a JEDEC test-board design and compared to ThermalCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

Package Thermal Performance

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_j - T_a}{P} \quad (1)$$

Where:

T_j = chip junction temperature

T_a = ambient temperature

P = device power dissipation

θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

JEDEC established the JC 15.1 committee, comprising industry representatives, to develop industry-standard specifications for thermal testing. The specifications include development of electrical test procedures, careful descriptions of appropriate test environments, guidelines for the design of thermal test chips, guidelines for thermal modeling, and specifications for component mounting. The specifications for component mounting are divided into a series for different package types. The specifications include test-board descriptions for low effective thermal-conductivity test boards with a single metal layer and high effective thermal-conductivity test boards with embedded solid copper planes simulating system power and ground planes.

In August 1996, the Electronics Industries Association released JESD 51-3 titled *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. The standard describes guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) as differentiated from a multilayer printed-circuit board (PCB), which might include power and ground planes. The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of the standard, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard methodology, thermal-impedance variations from test-board design should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimensions: 4.0 × 4.5 in. for packages > than 27 mm in length, 3.0 × 4.5 in. for packages ≤ 27 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to JESD 51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermCAL, a finite-difference thermal-modeling tool.

Eleven SLL packages were tested using a JEDEC test-board design and compared to ThermCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

Table 1. Package Comparison

PACKAGE TYPE (PINS, DESIGNATION)	DIE SIZE (mils)	θ_{JA} MEASURED (°C/W)	θ_{JA} MODELED (°C/W)	CHANGE (%)	PACKAGE	COUNT
56 DL	120 × 120	73.5	78.3	6.5		
20 DW	62 × 62	96.6	90.9	-5.9		
160 PCM	240 × 240	34.9	34.9	0		
52 PAH†	120 × 120	87.2	92.2	5.7		
52 PAH‡	120 × 120	72.7	75.2	3.4		
100 PZ	360 × 360	45	42.8	-4.9		
208 PDV	240 × 240	50.1	52.8	5.4		
48 DGG	120 × 120	89.1	93.5	4.9		
14 DGV	62 × 62	181.5	191.7	5.6		
48 DGV	62 × 186	92.9	89.9	-3.2		
100 PCA	240 × 240	33.3	34.9	4.8		

† S-pad leadframe
‡ Conventional leadframe

After the accuracy of the model results was established, all other SLL packages could be modeled. θ_{JA} data based on JESD 51-3 is available for all SLL leaded surface-mount packages (see Table 2). The data is grouped by package type with values of θ_{JA} shown at different airflow levels. Leadframe pad size and die size are shown.

Junction-to-case thermal-impedance (θ_{JC}) data is shown with the junction-to-ambient data. Measured θ_{JC} data was generated for the packages tested using the JEDEC PCB. Previously published values of θ_{JC} are used for packages not yet tested using the PCB designed to JESD 51-3.

56 DL	120 × 120	73.5	78.3	6.5	56 DL	120 × 120	73.5	78.3	6.5
20 DW	62 × 62	96.6	90.9	-5.9	20 DW	62 × 62	96.6	90.9	-5.9
160 PCM	240 × 240	34.9	34.9	0	160 PCM	240 × 240	34.9	34.9	0
52 PAH†	120 × 120	87.2	92.2	5.7	52 PAH†	120 × 120	87.2	92.2	5.7
52 PAH‡	120 × 120	72.7	75.2	3.4	52 PAH‡	120 × 120	72.7	75.2	3.4
100 PZ	360 × 360	45	42.8	-4.9	100 PZ	360 × 360	45	42.8	-4.9
208 PDV	240 × 240	50.1	52.8	5.4	208 PDV	240 × 240	50.1	52.8	5.4
48 DGG	120 × 120	89.1	93.5	4.9	48 DGG	120 × 120	89.1	93.5	4.9
14 DGV	62 × 62	181.5	191.7	5.6	14 DGV	62 × 62	181.5	191.7	5.6
48 DGV	62 × 186	92.9	89.9	-3.2	48 DGV	62 × 186	92.9	89.9	-3.2
100 PCA	240 × 240	33.3	34.9	4.8	100 PCA	240 × 240	33.3	34.9	4.8

Table 2. SLL Package Thermal-Impedance Data

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOIC										
14	D	MS-012	70 × 70	32 × 37	126.6	104	96.4	87.4	Modeled	46
16	D	MS-012	90 × 90	44 × 65	112.6	91.2	83.9	74.8	Modeled	42
20	DW	MS-013	90 × 110	62 × 62	96.6	82.2	77.7	71.5	Measured	38.3
24	DW	MS-013	140 × 160	84 × 122	80.7	53.7	47.5	40.7	Modeled	25
28	DW	MS-013	120 × 140	90 × 128	78.2	54.3	48.4	41.9	Modeled	
SSOP										
14	DB	MO-150	71 × 71	43 × 52	158	128.6	118.9	106.5	Modeled	47
16	DB	MO-150	83 × 91	51 × 61	130.8	105.9	97.3	86.5	Modeled	47
20	DB	MO-150	87 × 106	61 × 65	114.6	92	84	74.7	Modeled	45
24	DB	MO-150	87 × 106	74 × 91	104.2	83.5	76.3	67.5	Modeled	42
20	DBQ	MS-137	96 × 140	61 × 75	118.1	95.3	86.9	76.7	Modeled	46
24	DBQ	MS-137	96 × 140	61 × 75	113	92	84.1	74.6	Modeled	42
28	DL	MO-118	150 × 180	97 × 142	97	77.2	70.9	63.1	Modeled	
48	DL	MO-118	120 × 180	73 × 128	93.5	69.9	63.8	57.1	Modeled	26
56	DL	MO-118	150 × 220	120 × 120	73.5	62.3	59	54.6	Measured	27.3
PLCC										
28	FN	MS-018	300 × 348	214 × 319	70.9	58.8	52.7	46	Modeled	26.7
44	FN	MS-018	270 × 270	235 × 235	46.2	38.6	35.4	31.6	Modeled	22
68	FN	MS-018	325 × 325	280 × 280	39.3	33	30.5	27.6	Modeled	14.5
84	FN	MS-018	275 × 275	188 × 185	39.7	33.9	31.8	29.4	Modeled	11.9
QFP										
52	RC	MS-022	210 × 210	120 × 120	78.9	48.4	43.6	38.1	Modeled	20
80	PH		265 × 265	232 × 240	76.1	67.9	61.4	53.6	Modeled	15.1
132	PQ	MO-069	315 × 315	272 × 272	46.3	34.5	31.6	28.3	Modeled	9.8
144	PCM	MS-022	433 × 433	338 × 338	38.8	27.3	25.1	22.4	Modeled	14.5
160	PCM	MS-022	511 × 511	433 × 433	34.9	29.9	28.3	24.7	Measured	11.4
208	PPM	MO-143	413 × 413	268 × 268	36.7	30.4	28.1	26.7	Modeled	
TQFP										
52	PAH	MO-136	S-Pad	120 × 120	87.2	76.1	71.5	67	Measured	28.3
52	PAH	MO-136	3.5 × 3.5 mm	120 × 120	72.7	62.6	59.2	53.8	Measured	24.0
64	PM	MO-136	6.75 × 6.75 mm	235 × 235	66.9	53.6	47.6	40.6	Modeled	10.4
64	PAG	MO-136	S-Pad	240 × 240	58.2	48.8	45.2	40.3	Measured	22.6
80	PN	MO-136	S-Pad	240 × 240	61.5	52.8	49.3	44.6	Measured	26.4
100	PZ	MO-136	S-Pad	360 × 360	45	38.3	35.3	27.9	Measured	7.6
100	PZ	MO-136	S-Pad	240 × 240	50.1	42.7	40.4	36.8	Measured	21.1
100	PCA	MO-136	6.5 × 6.5 mm	240 × 240	33.3	24.7	21.8	19.2	Measured	4.3
120	PCB	MO-136	6.5 × 6.5 mm	240 × 240	28.1	22.3	21	18	Modeled	3.3
144	PGE	MO-136	342 × 350	378 × 378	48.3	39.1	35.5	31	Modeled	9.9
208	PDV	MO-136	S-Pad	240 × 240	50.1	43.63	40.9	37.3	Measured	9.9

Table 2. SLL Package Thermal-Impedance Data (Continued)

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOP										
14	NS	EIAJ-TYPE-II	79 × 87	55 × 57	127.1	103.7	95.5	85.2	Modeled	95
16	NS	EIAJ-TYPE-II	87 × 142	76 × 86	111.3	89.3	81.4	71.5	Modeled	95
20	NS	EIAJ-TYPE-II	87 × 118	60 × 77	100.3	82.8	76.2	68	Modeled	90
TSSOP										
14	PW	MO-153	71 × 71	48 × 53	169.8	146.7	136	121.7	Modeled	35
16	PW	MO-153	104 × 104	56 × 76	148.9	127.9	117.6	103.9	Modeled	35
20	PW	MO-153	102 × 106	53 × 69	128	110.6	101.9	90.8	Modeled	34
24	PW	MO-153	94 × 140	74 × 91	119.9	98.8	90.6	80	Modeled	33
48	DGG	MO-153	4.6 × 3.2 mm	120 × 120	89.1	78.5	75.1	69.4	Measured	25.2
56	DGG	MO-153	3.94 × 5.08 mm	132 × 176	81.2	72.8	65.8	57.9	Modeled	13
64	DGG	MO-153	5.7 × 3.6 mm	120 × 120	72.9	63.3	61.8	57.1	Measured	21.3
TVSOP										
14	DGV	MO-194	75 × 75	62 × 62	181.5	165.8	159.5	150.4	Measured	66.7
16	DGV	MO-194	75 × 75	65 × 65	179.6	153.2	141.7	126.3	Modeled	
20	DGV	MO-194	104 × 104	94 × 94	146.1	122.3	111.6	97.4	Modeled	
24	DGV	MO-194	104 × 104	94 × 94	138.6	116.2	106.2	93.2	Modeled	
48	DGV	MO-194	100 × 240	62 × 186	92.9	80.9	77.1	71	Measured	27.2
56	DGV	MO-194	100 × 274	90 × 262	85.9	64.6	57.1	48.4	Modeled	
80	DBB	MO-194	100 × 224	93 × 203	105.6	78.4	71.8	63.7	Modeled	
PDIP (assumes zero trace length)										
8	P	MS-001			104					41
14/16	N	MS-001			78					32
20	N	MS-001			67					33
24	NT	MS-001			67					25
		BGA								
256	GFN	MO-151			42				ANAM data	6.2
388	GFW	MO-151			18.9				Model data	



Figure 1. Input Waveform

Table 2 shows the switching of each pin for AHC devices. Once the C_{PD} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Although a C_{PD} value is not provided for ABT and LVT, the I_{CC} versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of $nA/(MHz \times bit)$, which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

Power Calculation

Reduction of power consumption makes a device more robust and reliable. When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL} , I_{CCH} , or I_{CCZ}), while a CMOS device has a single value for I_{CC} . These values can be found in the individual data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched completely off. This value, known as ΔI_{CC} , also is provided in the data sheet.

Due to the high operating frequencies, there is a strict limit on power consumption in computer systems. Therefore, allowable power consumption for each device on a board must be minimized. Power calculations are made to determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculation also can determine the maximum reliable operating frequency.

There are two components that establish the amount of power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd} , which is listed in the data sheet and is obtained using equations 2 and 3:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad (2)$$

$$C_{L(eff)} = C_L \times N_{sw} \times \frac{f_o}{f_I} \quad (3)$$

To explain the C_{pd} and the method of calculating dynamic power, see Table 3, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 3 are:

V = V_{CC} (5 V)

G = ground (0 V)

1 = high logic level = V_{CC} (5 V)

0 = low logic level = ground (0 V)

X = don't care: 1 or 0, but not switching

C = 50% duty cycle input pulse (1 MHz) (see Figure 1)

D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 1)

S = standard ac output load (50 pF to GND)

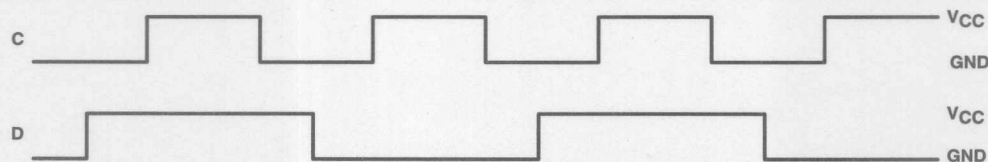


Figure 1. Input Waveform

Table 3 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Although a C_{pd} value is not provided for ABT and LVT, the I_{CC} versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of mA/(MHz \times bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

Table 3. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN NO.																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal

‡ All bits switching

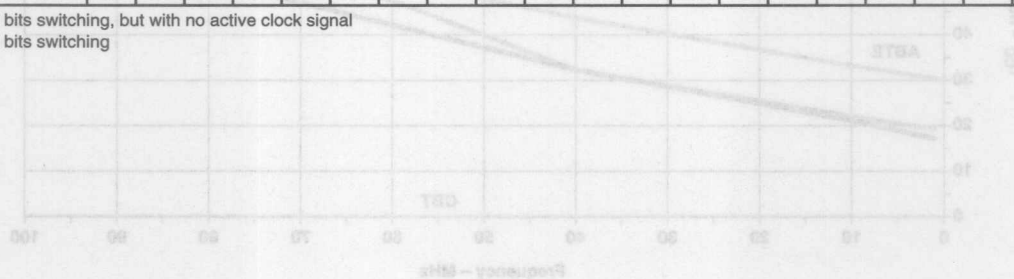


Figure 2. Power Consumption With a Single Output Switching

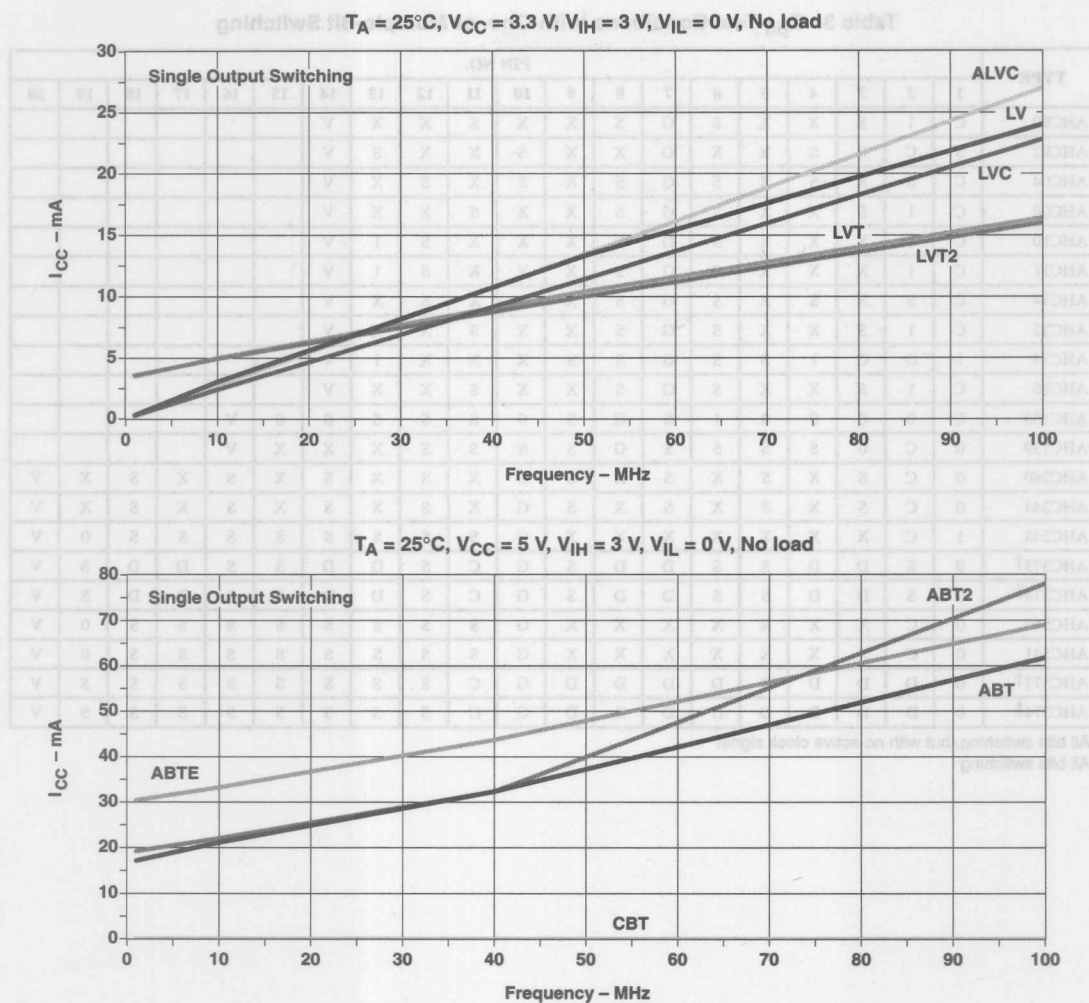


Figure 2. Power Consumption With a Single Output Switching

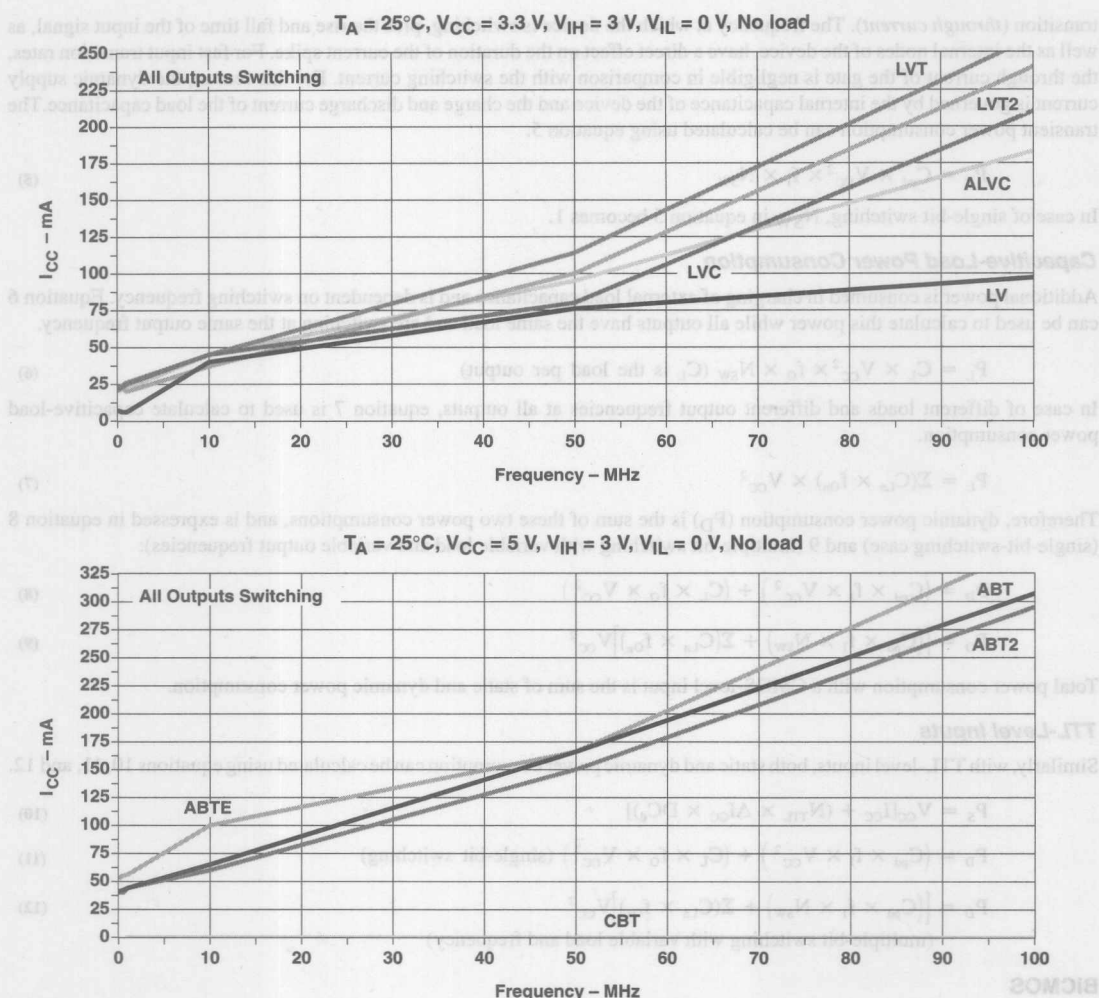


Figure 3. Power Consumption With All Outputs Switching

CMOS

CMOS-Level Inputs

Static power consumption can be calculated using equation 4.

$$P_s = V_{CC} \times I_{CC} \quad (4)$$

The dynamic power consumption of a CMOS device is calculated by adding the transient power consumption and capacitive-load power consumption.

Transient Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic

transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance. The transient power consumption can be calculated using equation 5.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{SW} \quad (5)$$

In case of single-bit switching, N_{SW} in equation 5 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 6 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{SW} \quad (C_L \text{ is the load per output}) \quad (6)$$

In case of different loads and different output frequencies at all outputs, equation 7 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2 \quad (7)$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 8 (single-bit-switching case) and 9 (multiple-bit switching with variable load and variable output frequencies):

$$P_D = (C_{pd} \times f_I \times V_{CC}^2) + (C_L \times f_O \times V_{CC}^2) \quad (8)$$

$$P_D = [(C_{pd} \times f_I \times N_{SW}) + \Sigma(C_{Ln} \times f_{On})] V_{CC}^2 \quad (9)$$

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 10, 11, and 12.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad (10)$$

$$P_D = (C_{pd} \times f_I \times V_{CC}^2) + (C_L \times f_O \times V_{CC}^2) \quad (\text{single-bit switching}) \quad (11)$$

$$P_D = [(C_{pd} \times f_I \times N_{SW}) + \Sigma(C_{Ln} \times f_{On})] V_{CC}^2 \quad (\text{multiple-bit switching with variable load and frequency}) \quad (12)$$

BICMOS

Static Power

$$P_S = V_{CC} \left\{ DC_{en} \left[\left(N_H \times \frac{I_{CCH}}{N_T} \right) + \left(N_L \times \frac{I_{CCL}}{N_T} \right) \right] + (1 - DC_{en}) I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d) \right\} \quad (13)$$

Where:

$$\Delta I_{CC} = 0 \text{ for bipolar devices}$$

NOTE:

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Equation 13 becomes:

$$P_S = V_{CC} \left[\left(N_H \times \frac{I_{CCH}}{N_T} \right) + \left(N_L \times \frac{I_{CCL}}{N_T} \right) \right] \quad (14)$$

NOTE:

If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2 N_T)$, P_S becomes:

$$P_S = \left(\frac{V_{CC}}{2} \right) (I_{CCH} + I_{CCL}) \quad (15)$$

Dynamic Power

$$P_D = (DC_{en} \times N_{sw} \times V_{CC} \times f \times I_{CCD}) \text{ Condition is } 50 \text{ pF} \parallel 500 \Omega \quad (16)$$

I_{CCD} is calculated with $50 \text{ pF} \parallel 500 \Omega$ and given number of outputs switching.

NOTE:

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{sw} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50 \text{ pF}) + DC_{en} \times N_{sw} \times V_{CC} \times f \times I_{CCD} \quad (17)$$

I_{CCD} is calculated with $50 \text{ pF} \parallel 500 \Omega$ and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500Ω in most load circuits for outputs in the data sheet). This power is very small but must be included in the dynamic power consumption calculation. Equation 18 is used to calculate this power consumption.

$$P_{Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad (18)$$

NOTE:

Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D_TOT} = P_D + P_{Res} \quad (19)$$

Finally, total power consumption can be calculated as:

$$P_{Total} = P_{D_TOT} + P_S \quad (20)$$

Where:

- V_{CC} = supply voltage (V)
- I_{CC} = power-supply current (A) (from the data sheet)
- I_{CCL} = power-supply current when outputs are in low state (A) (from the data sheet)
- I_{CCH} = power-supply current when outputs are in high state (A) (from the data sheet)
- I_{CCZ} = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
- ΔI_{CC} = power-supply current when one input is at a TTL level (A) (from the data sheet)
- DC_{en} = % duty cycle enabled ($50\% = 0.5$)
- DC_d = % duty cycle of the data ($50\% = 0.5$)
- N_H = number of outputs in high state
- N_L = number of outputs in low state
- N_{sw} = total number of outputs switching
- N_T = total number of outputs
- N_{TTL} = number of inputs driven at TTL levels
- f_I = input frequency (Hz)
- f_O = output frequency (Hz)
- f = operating frequency (Hz)

V_{OH} = output voltage in high state (V)
 V_{OL} = output voltage in low state (V)
 C_L = external-load capacitance (F)
 I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz \times bit)

$C_{L(eff)}$ = effective-load capacitance (F)
 f_O/f_I = ratio of output and input frequency (Hz)
 P_T = transient power consumption
 P_D = dynamic power consumption
 P_S = static power consumption
 P_{Res} = power consumption due to output resistance
 P_{D_TOT} = total dynamic power consumption
 P_{Total} = total power consumption

C_{PD} = dynamic power dissipation capacitance (F)
 P_L = capacitive-load power consumption
 Σ = sum of n different frequencies and loads at n different outputs
 f_{On} = all different output frequencies at each output numbered 1 through n (Hz)
 C_{Ln} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device might not function properly.

Benefits of Minimizing Power Consumption

Power consumption can be minimized in a number of ways. DC power consumption can be reduced to leakage by using only CMOS logic, as opposed to bipolar and BiCMOS logic. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and the frequency at which the logic is clocked. Supply voltage tends to be a system design consideration, and low-power systems use 1.5-V to 3.3-V supplies.

Power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Reliability Implications

The integrated-circuit component power dissipation during operation elevates the device junction temperature. The thermal impedance (θ_{JA} or k-factor) of a device package is defined as the increase in the junction temperature, above ambient temperature, due to the device power dissipation. Thermal impedance is measured in degrees Celsius per watt. Thermal characteristics of a device package are commonly described using two indices, Q_{JA} (junction to ambient) and Q_{JC} (junction to case). Controlling the junction temperature within a desired range is critical for proper device functionality and long-term reliability.

Table 4, based on long-term sustained temperatures, shows the relationship between junction temperature and predicted failure rate.

Table 4. Junction Temperature Versus 100,000-Hour Predicted Failure Rate

JUNCTION TEMPERATURE (°C)	FAILURE RATE (%)
100	0.02
110	1
120	11
130	46
140	80
150	96

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failures.

Thermal Definitions

<i>Heat</i>	A form of energy associated with the motion of atoms or molecules in solids, and capable of being transmitted through solid and fluid media by conduction, through fluid media by convection, and through empty space by radiation
<i>Conduction Heating</i>	The most commonly recognized form of heat transfer. Metal materials are good conductors of heat and can be quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal-conductivity number, the more quickly heat transfer, by means of conduction, occurs. Leadframes are the primary media for conduction heating in plastic-encapsulated devices; however, mold compound materials play a major role in this type of heat transference.
<i>Convection Heating</i>	The heat transfer by fluid motion between regions of unequal density that result from nonuniform heating. This type of heat transfer is most commonly seen when air is forced across a heated surface, resulting in the cooling of the heat source. Heat is transferred to the air by means of convection heating. The rate of heat transfer depends on the surface area of the heat source and the velocity and physical properties of the airflow. When a device package is generating heat through normal operation, the device can be cooled by applying a constant airflow across the surface of the package.
<i>Radiation</i>	Radiant heat transfer occurs between two objects separated within a vacuum.
<i>Ambient Temperature</i>	The temperature of the surrounding air, usually used as a reference point to calculate the junction or case temperature. This temperature is measured at some specific distance from the device.
<i>Case Temperature</i>	The temperature on the package surface measured at the center of the top of the package
<i>Junction Temperature</i>	The temperature of the die inside the device package

Acknowledgment

The authors of this report are David Holmgreen, Doug Romm, Abul Sarwar, and Ron Eller. The thermal-model program, ThermCAL, was developed by Darvin Edwards.

References

- 1 Electronic Industries Association, EIA/JEDEC Std JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, August 1996.
- 2 Darvin Edwards, "Thermal Analysis Using FEA (v1.1)," November 1991.
- 3 Darvin Edwards, "Development of JEDEC Standard Thermal Measurement Test Boards."

Failure Rate (%)	Junction Temperature (°C)
0.02	100
1	110
11	120
40	130
80	140
98	150

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failure.

Thermal Definitions

Heat A form of energy associated with the motion of atoms or molecules in solids, and capable of being transmitted through solid and fluid media by conduction, through fluid media by convection, and through empty space by radiation.

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Radiation Radiation heat transfer occurs between two objects separated within a vacuum.

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Case Temperature The temperature on the package surface measured at the center of the top of the package.

Junction Temperature The temperature of the inside the device package.

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Mechanical Data

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ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading, regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.

EXAMPLE: SN 74LVTH162244 DGG R

Prefix

SN = Standard prefix
SNJ = Compliant to MIL-PRF-38535 (QML)

Unique Circuit Description

MUST CONTAIN EIGHT TO FIFTEEN CHARACTERS

Examples: 74LVTH125
74LVTH16952
74LVTH162541

Package

MUST CONTAIN ONE TO THREE LETTERS

D, DW = plastic small-outline package
DB, DL = plastic shrink small-outline package
DCK = plastic small-outline transistor package
DGG, PW = plastic thin shrink small-outline package
DGV = plastic thin very small-outline package
FK = ceramic chip carrier
J, JT = ceramic dual-in-line package
W, WD = ceramic flat package
(from pin-connection diagram on individual data sheet)

Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

Blank = Not taped and reeled
R = Reeled product†

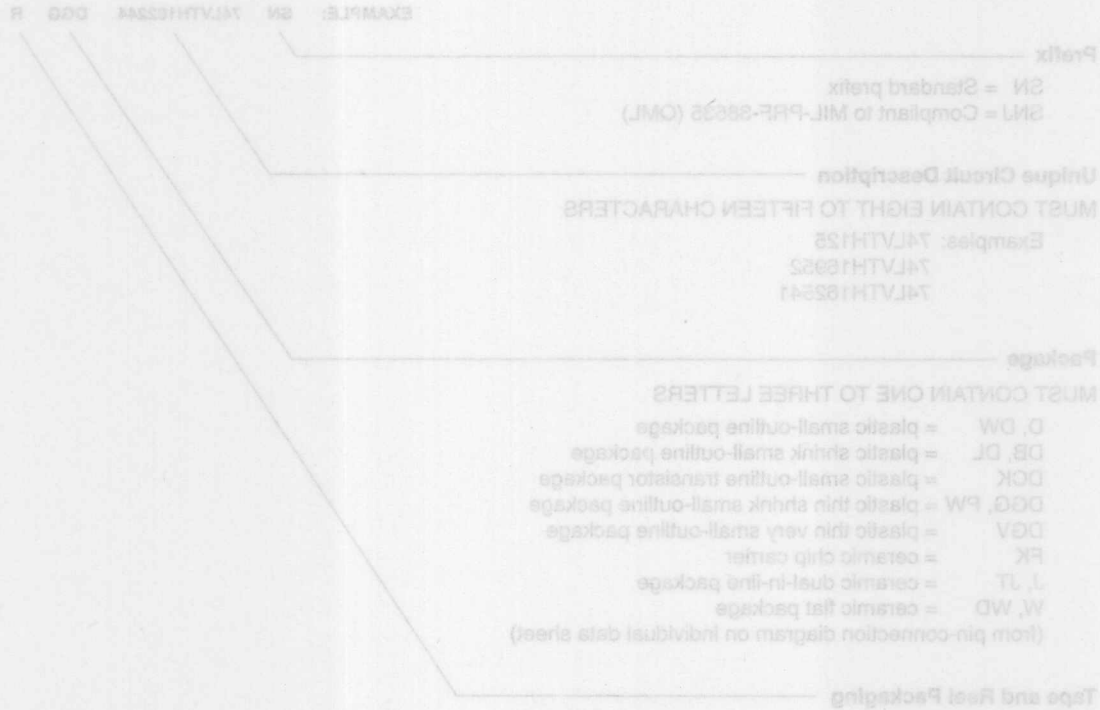
† All reeled material previously designated LE continues to be reeled left embossed, but an R designator is used.



ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading, regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.



† All unused material previously designated as "obsolete" continues to be needed for embedded, but an R designation is used.

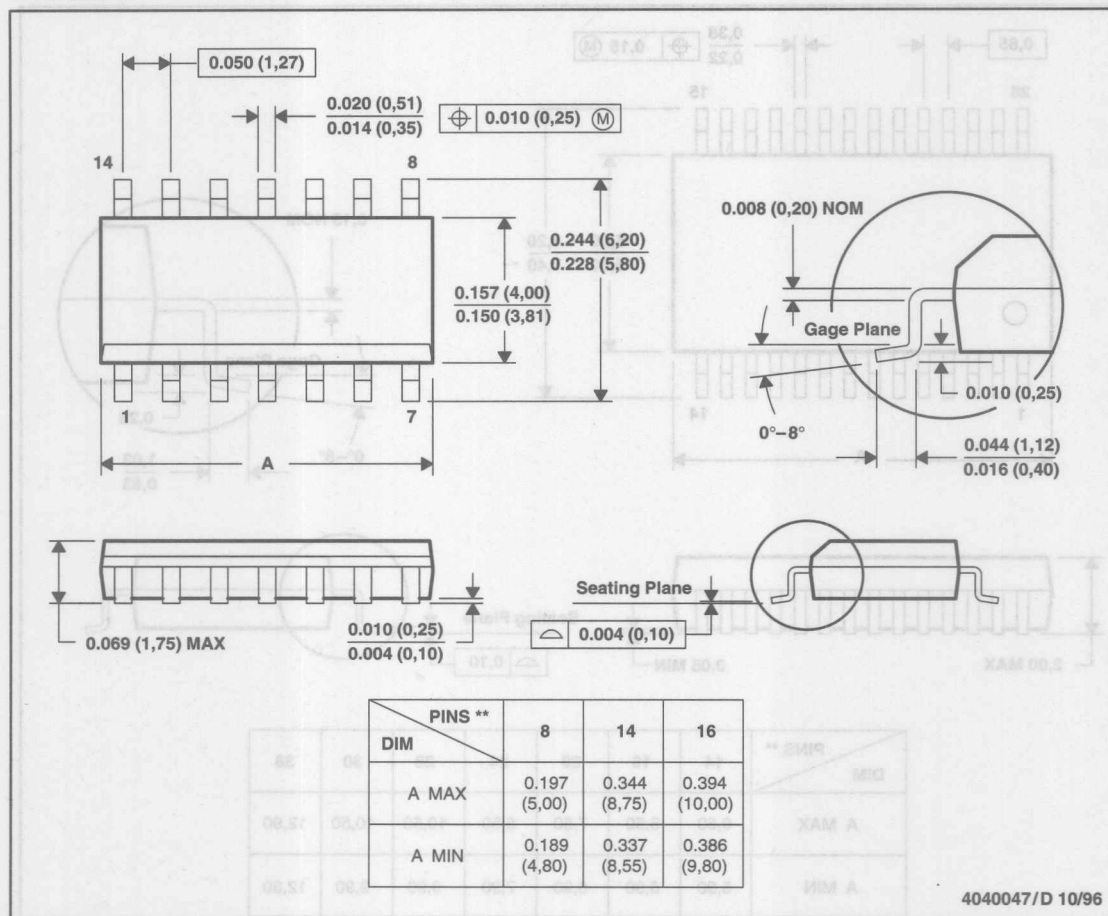


POST OFFICE BOX 655500 • DALLAS, TEXAS 75265

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012

TEXAS
INSTRUMENTS

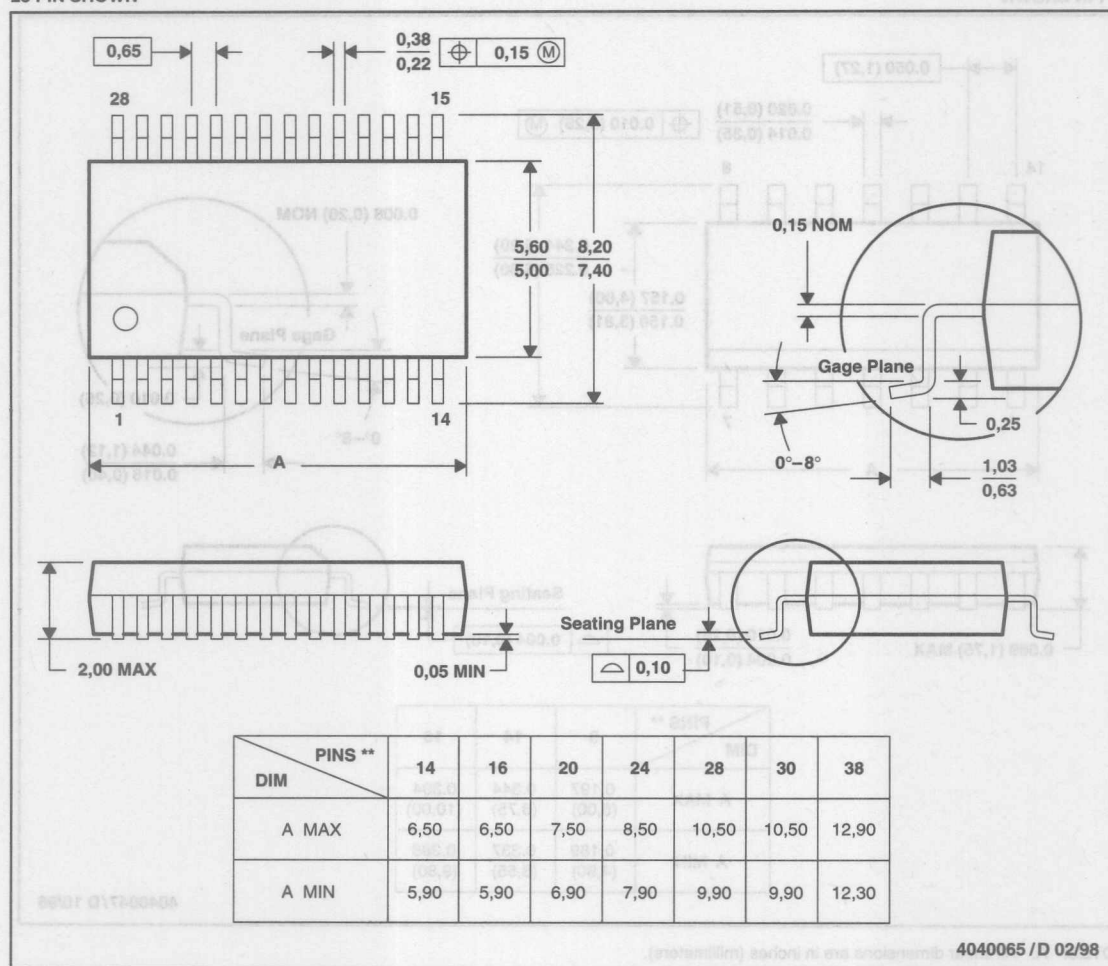
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MECHANICAL DATA

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

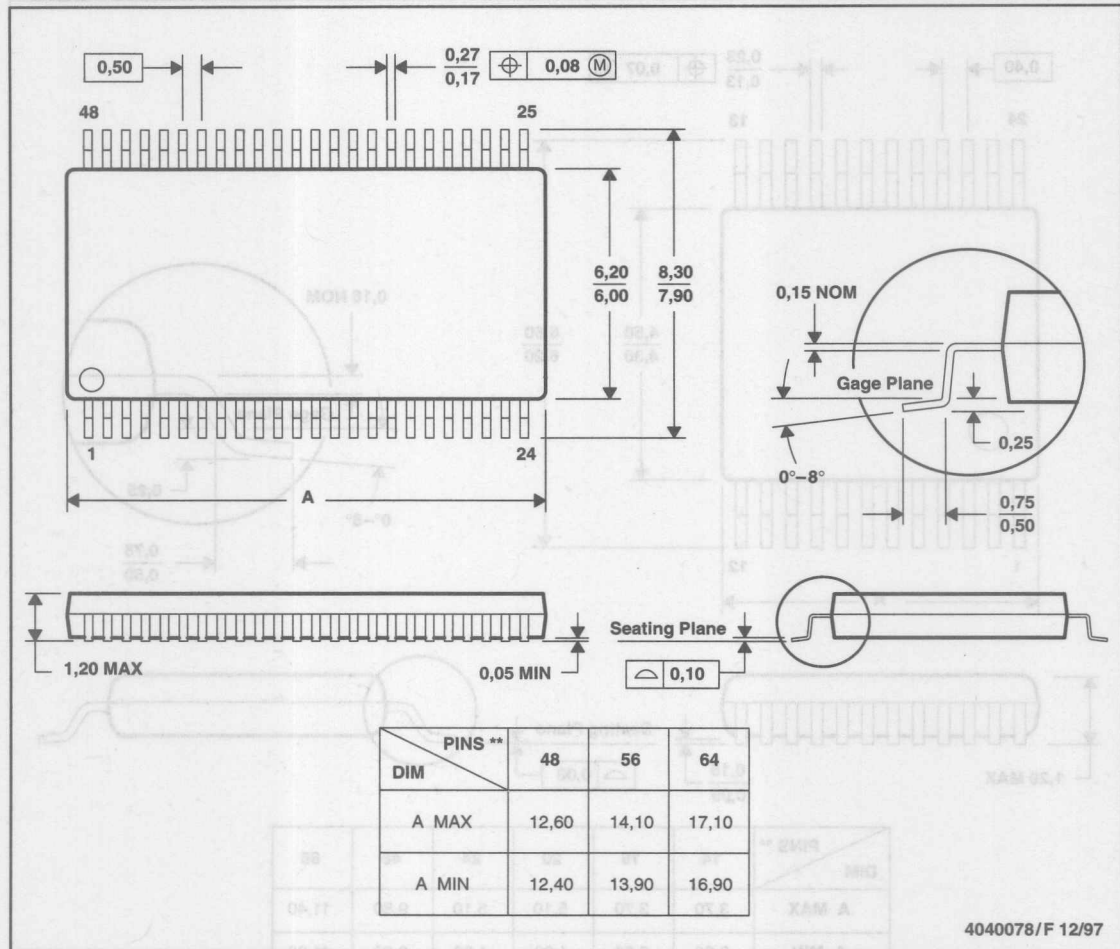


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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PIN SHOWN



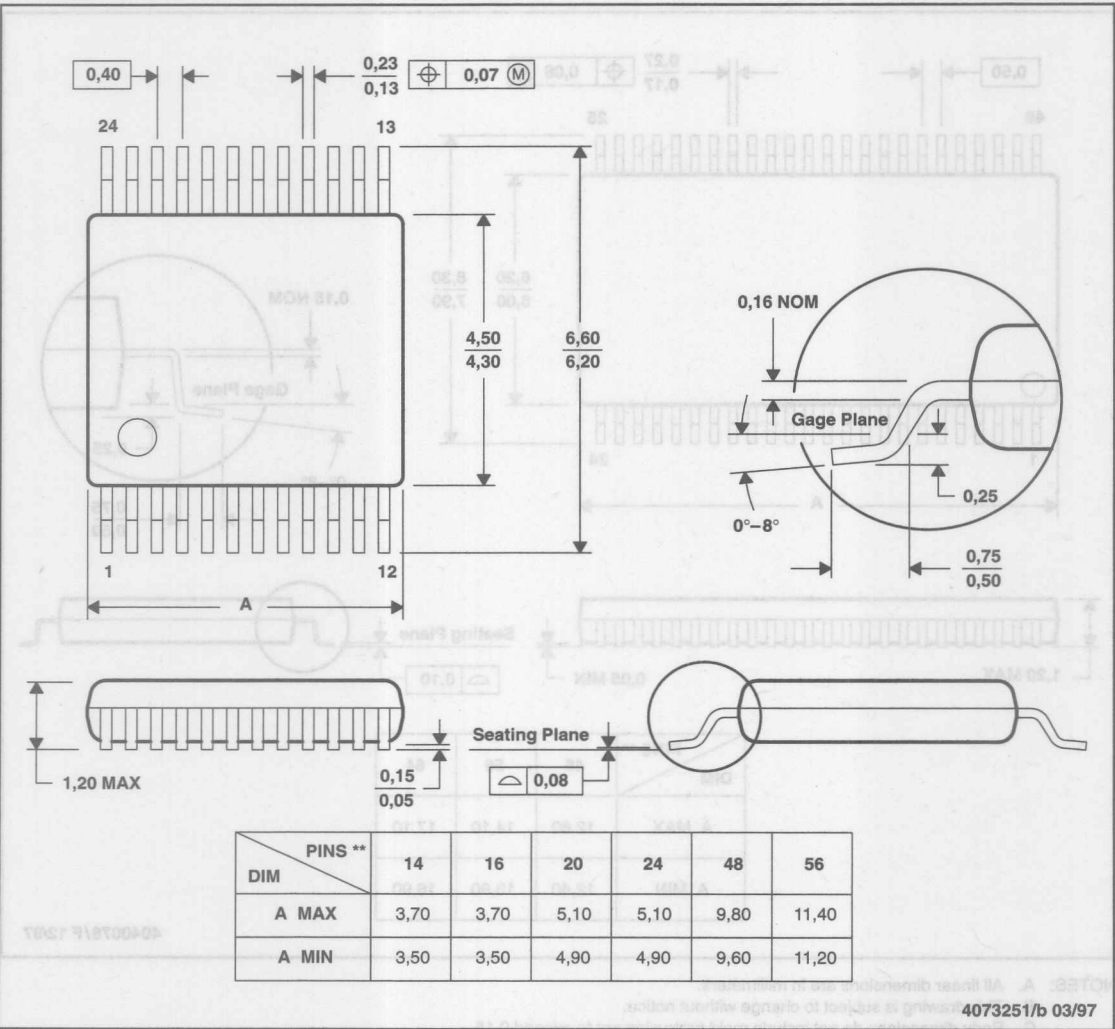
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

MECHANICAL DATA

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. The 24 and 48 pins falls within JEDEC MO-153 and the 14, 16, 20, and 56 pins falls within JEDEC MO-194.



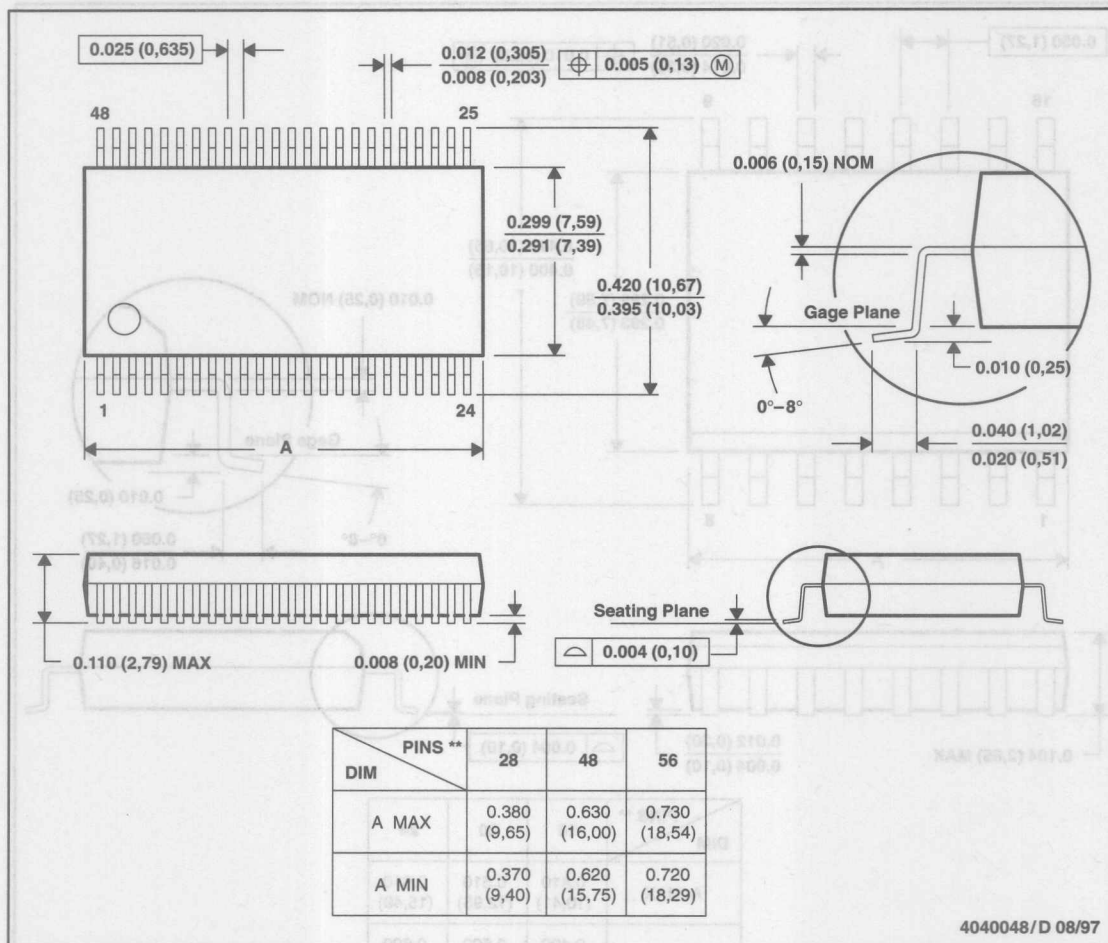
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MECHANICAL DATA

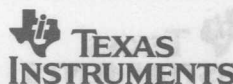
DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



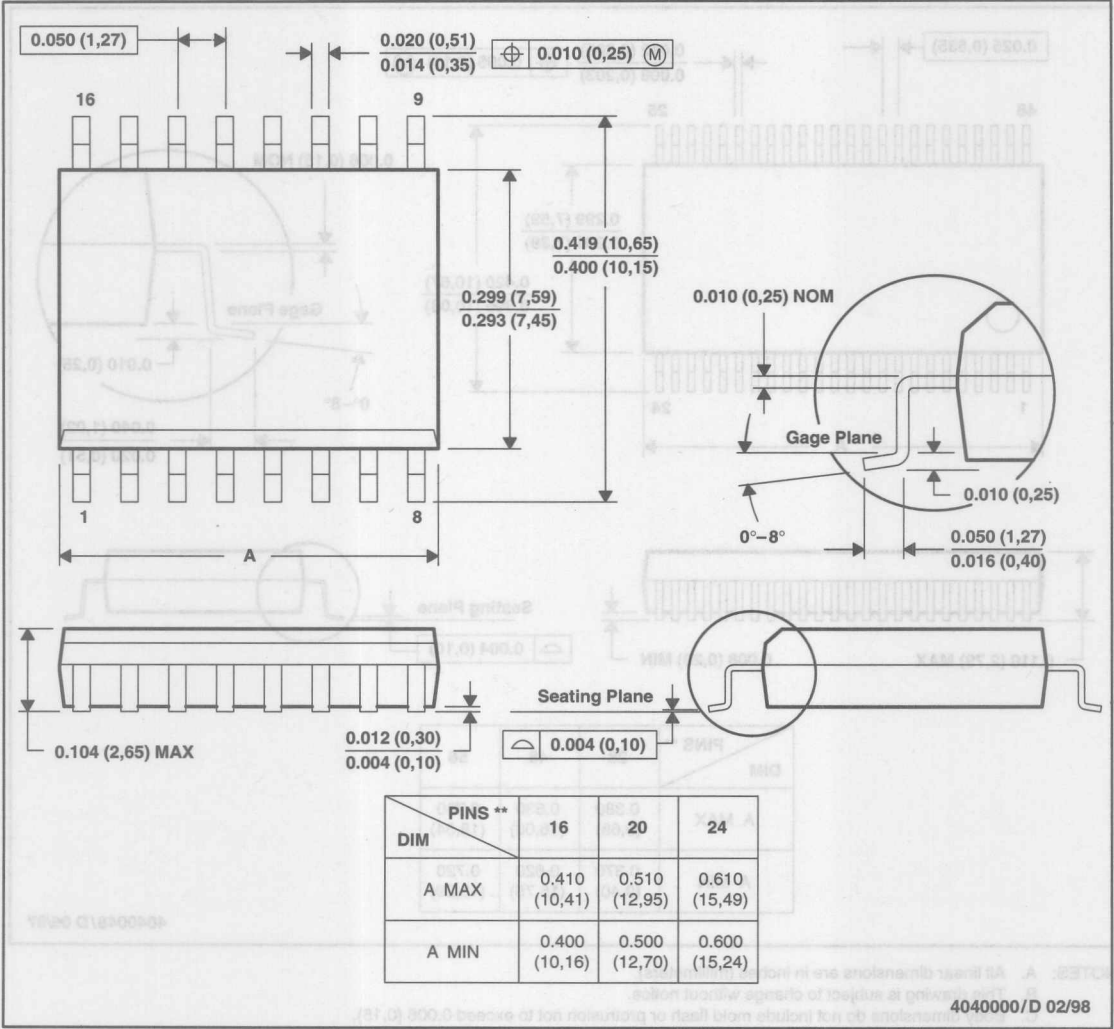
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118



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MECHANICAL DATA

DW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE 16 PIN SHOWN



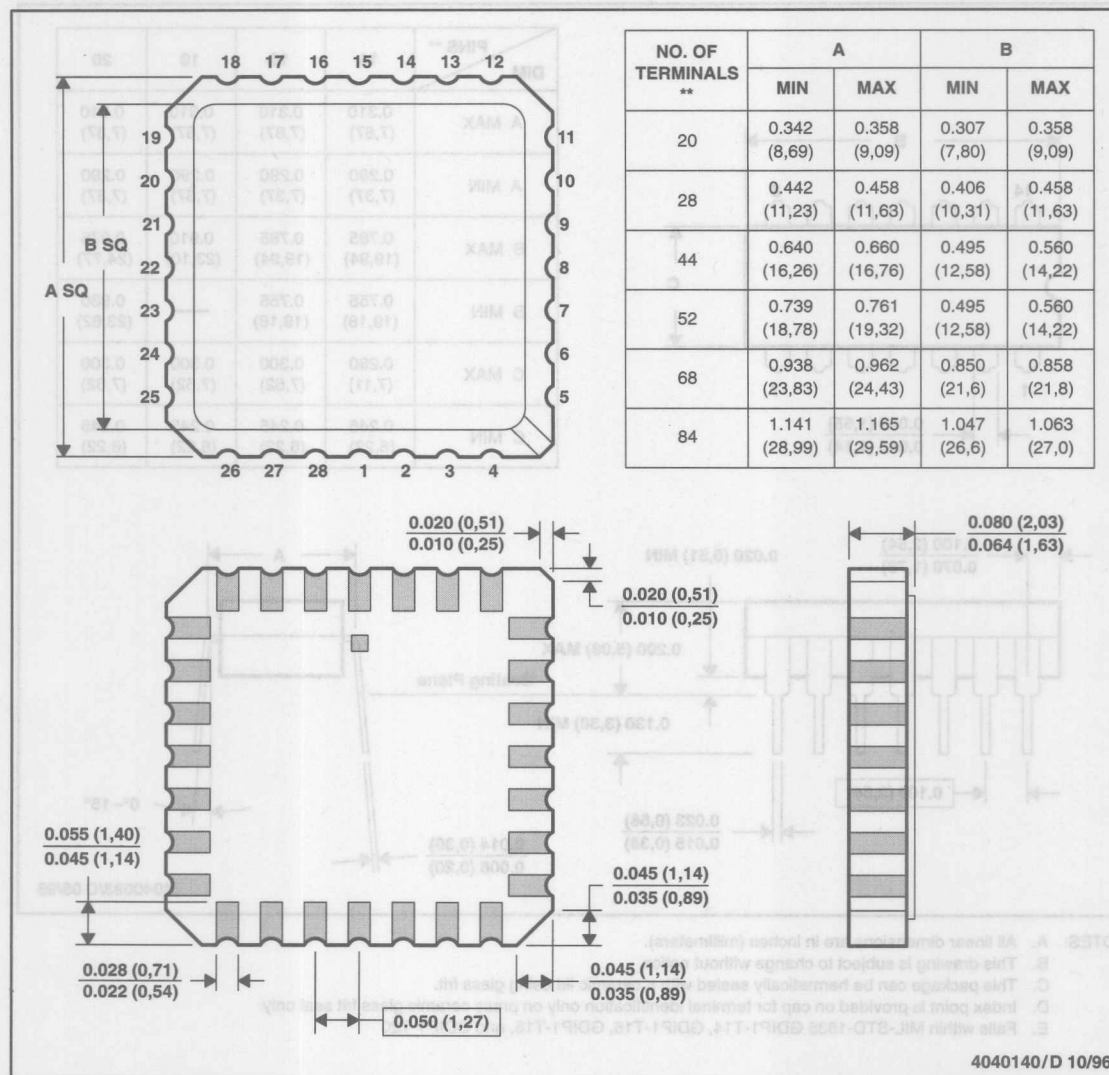
- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

**TEXAS
INSTRUMENTS**

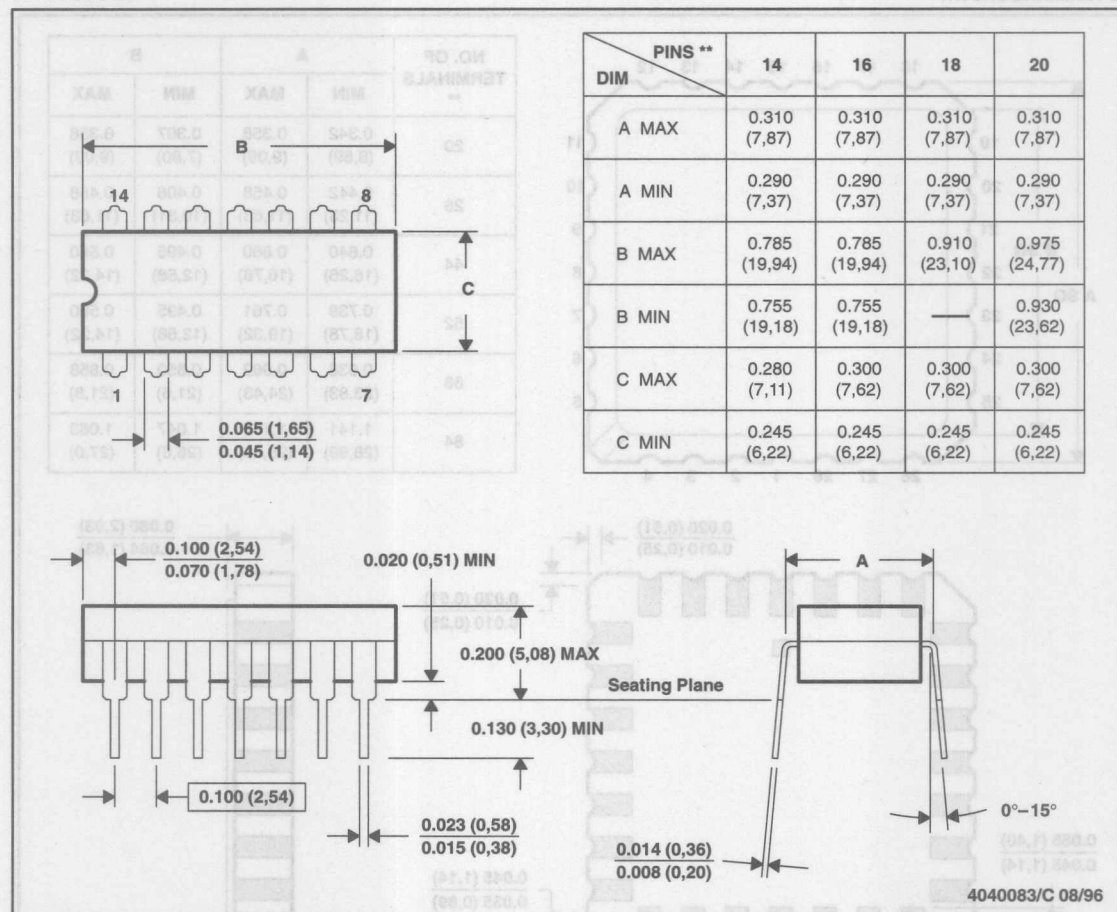
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MECHANICAL DATA

J (R-GDIP-T**) CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, and GDIP1-T20

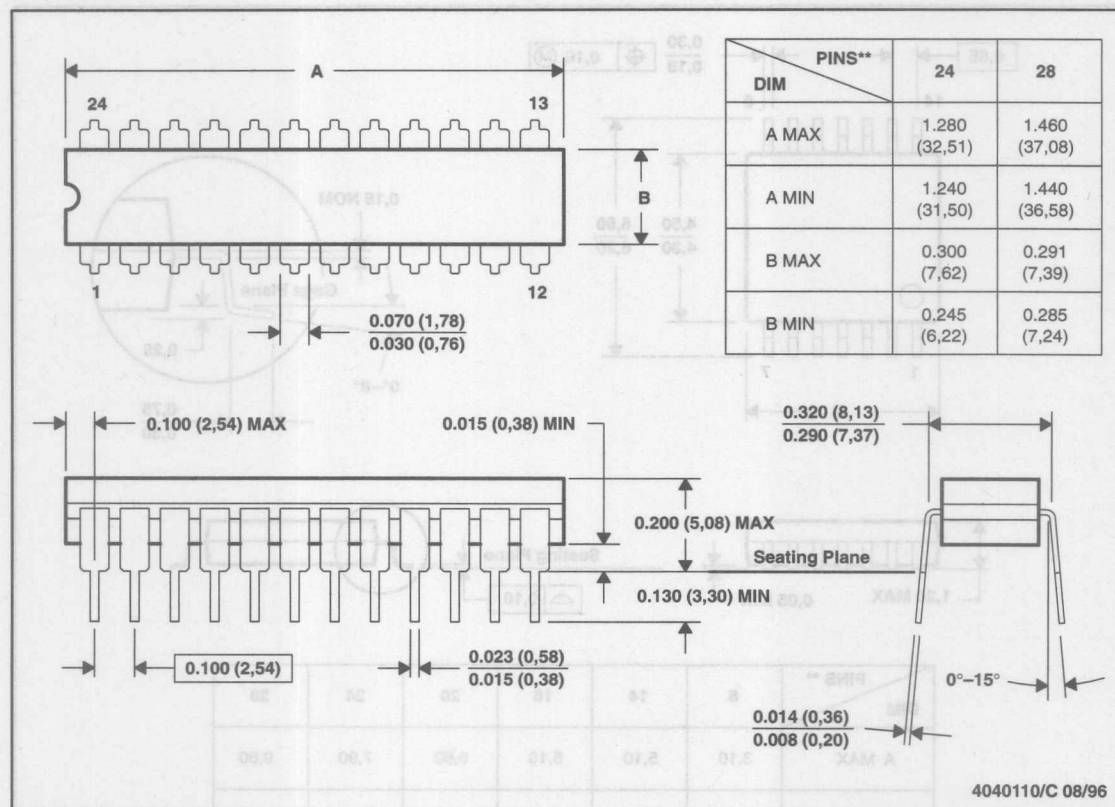


MECHANICAL DATA

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP-T24, GDIP-T28 and JEDEC MO-058 AA, MO-058 AB.

**TEXAS
INSTRUMENTS**

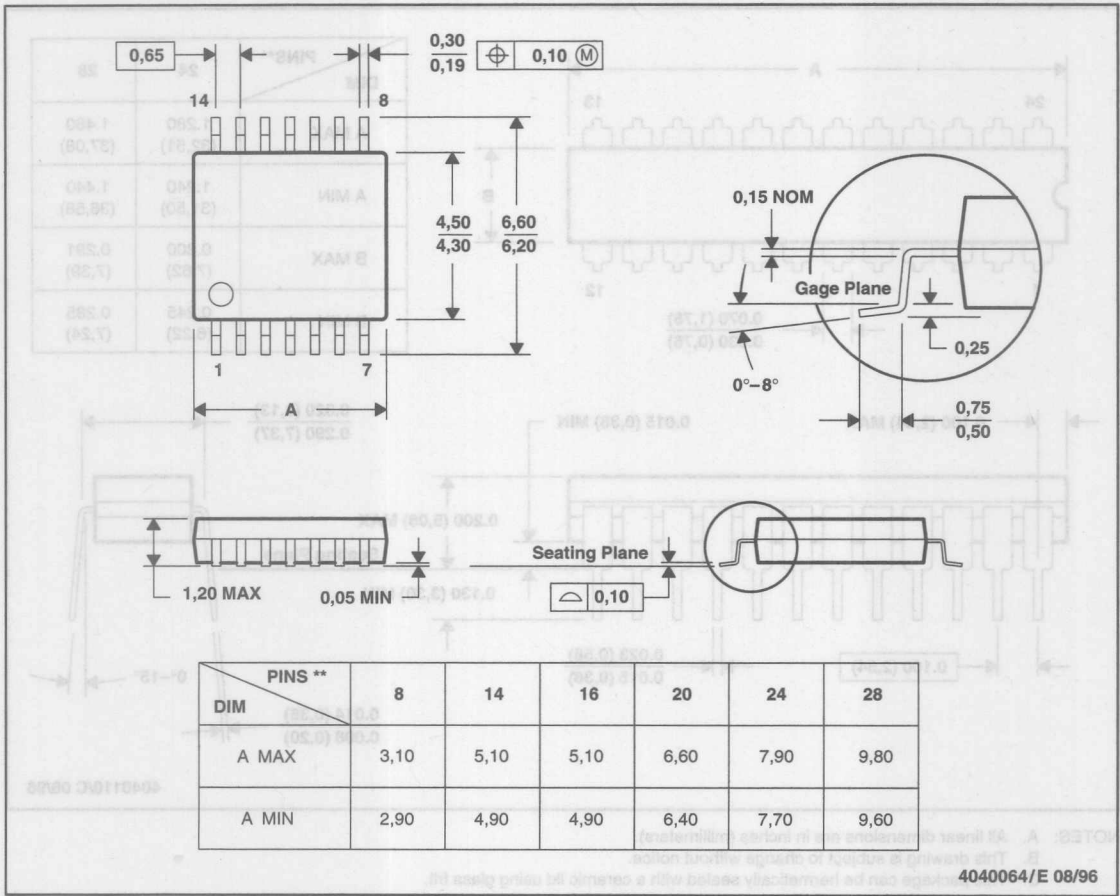
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MECHANICAL DATA

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

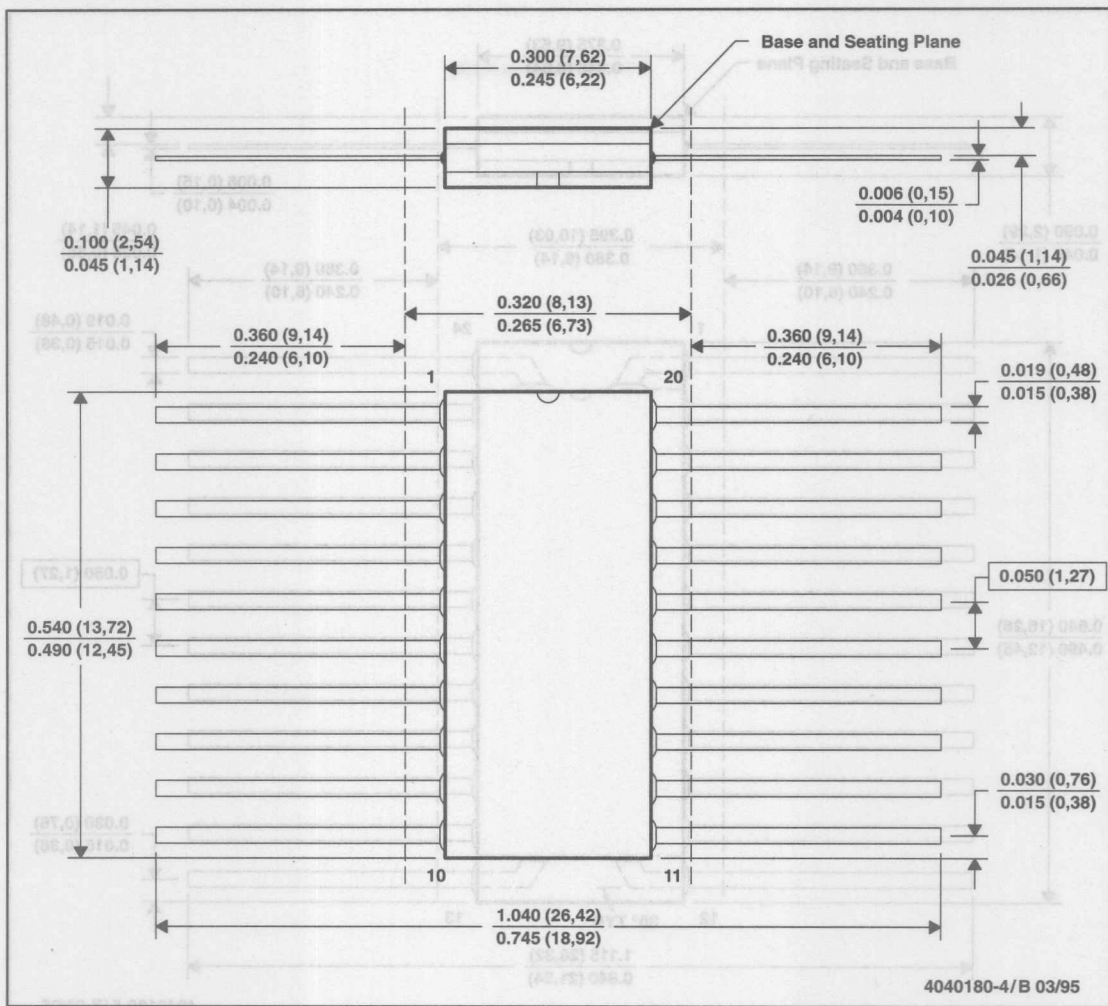
14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-153



CERAMIC DUAL FLATPACK

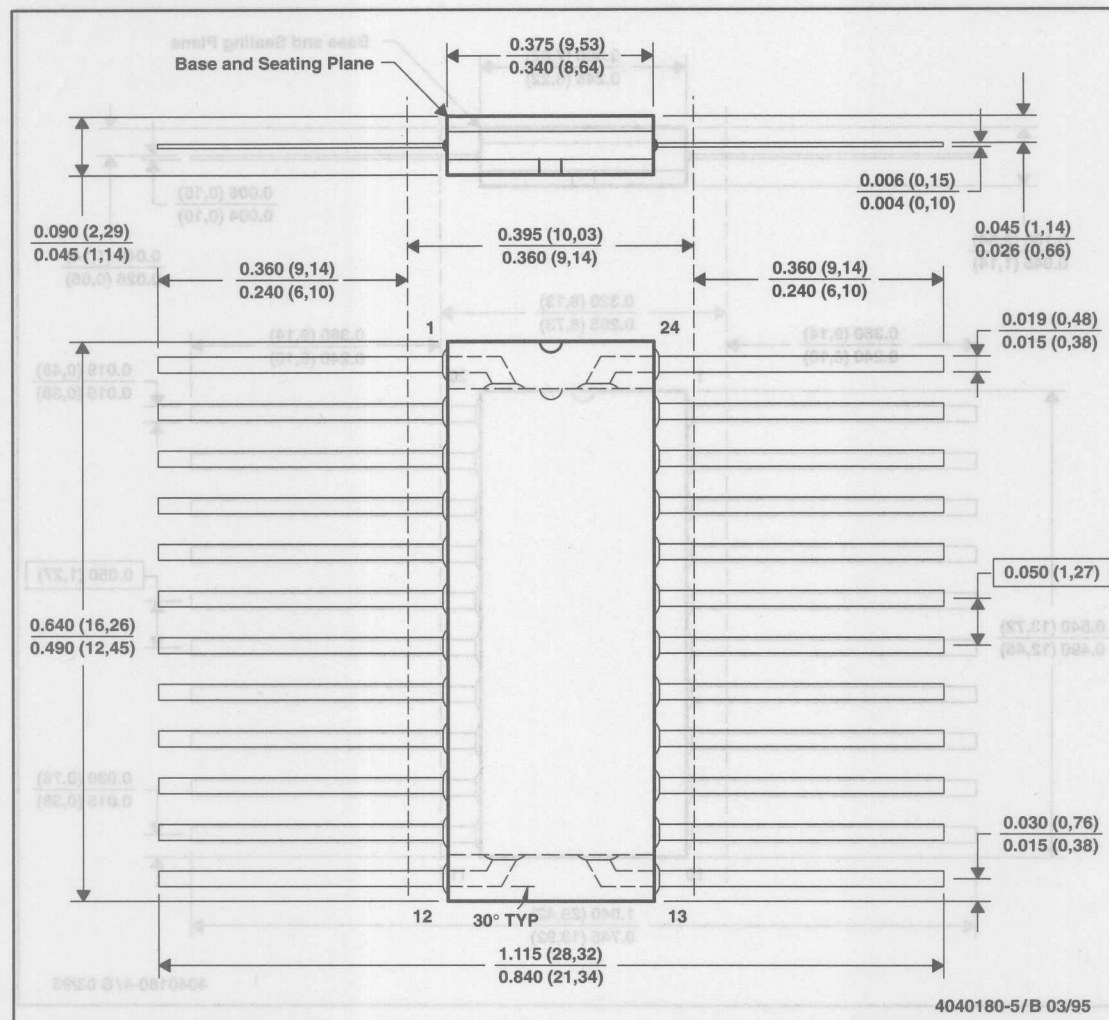


- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDPP2-F20

MECHANICAL DATA

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

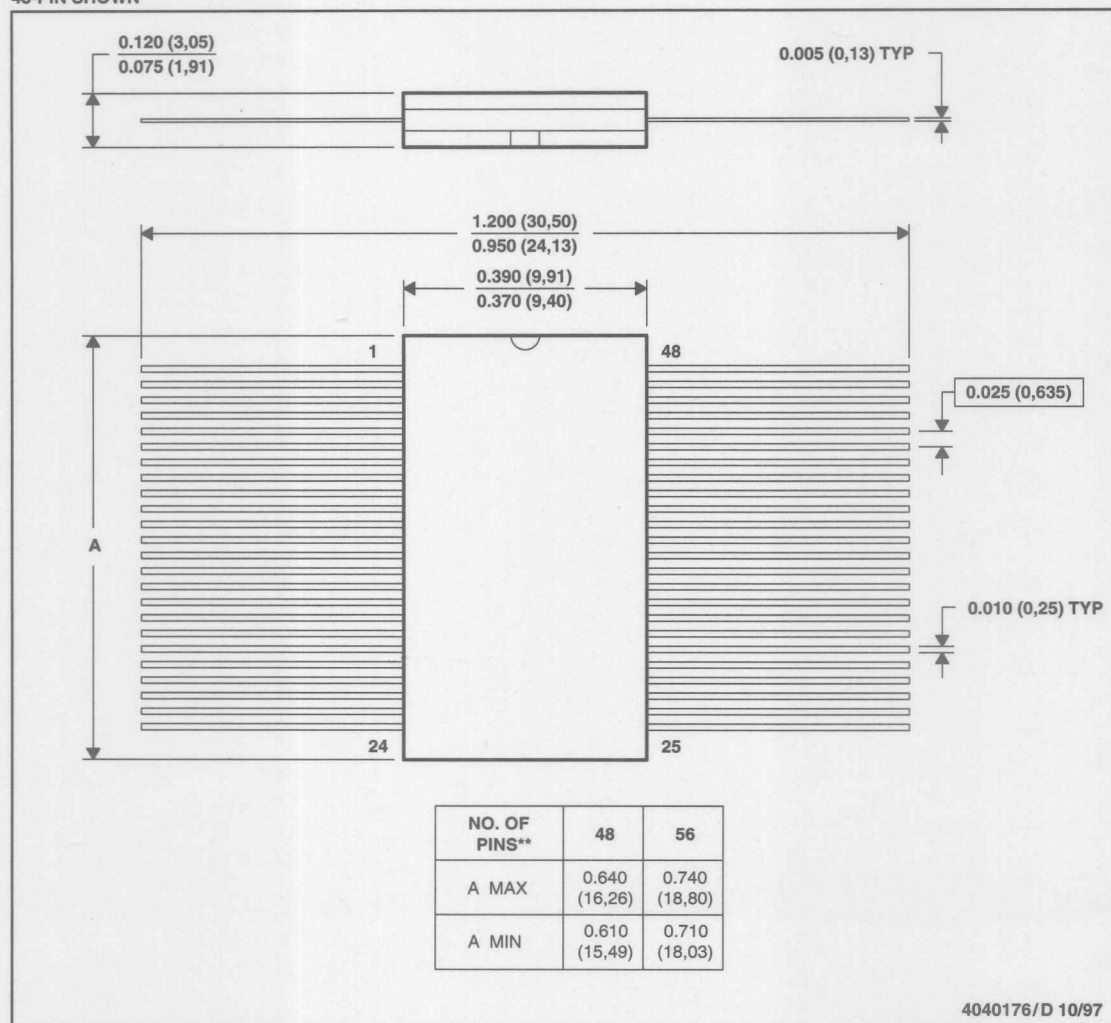
**TEXAS
INSTRUMENTS**

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WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48-PIN SHOWN

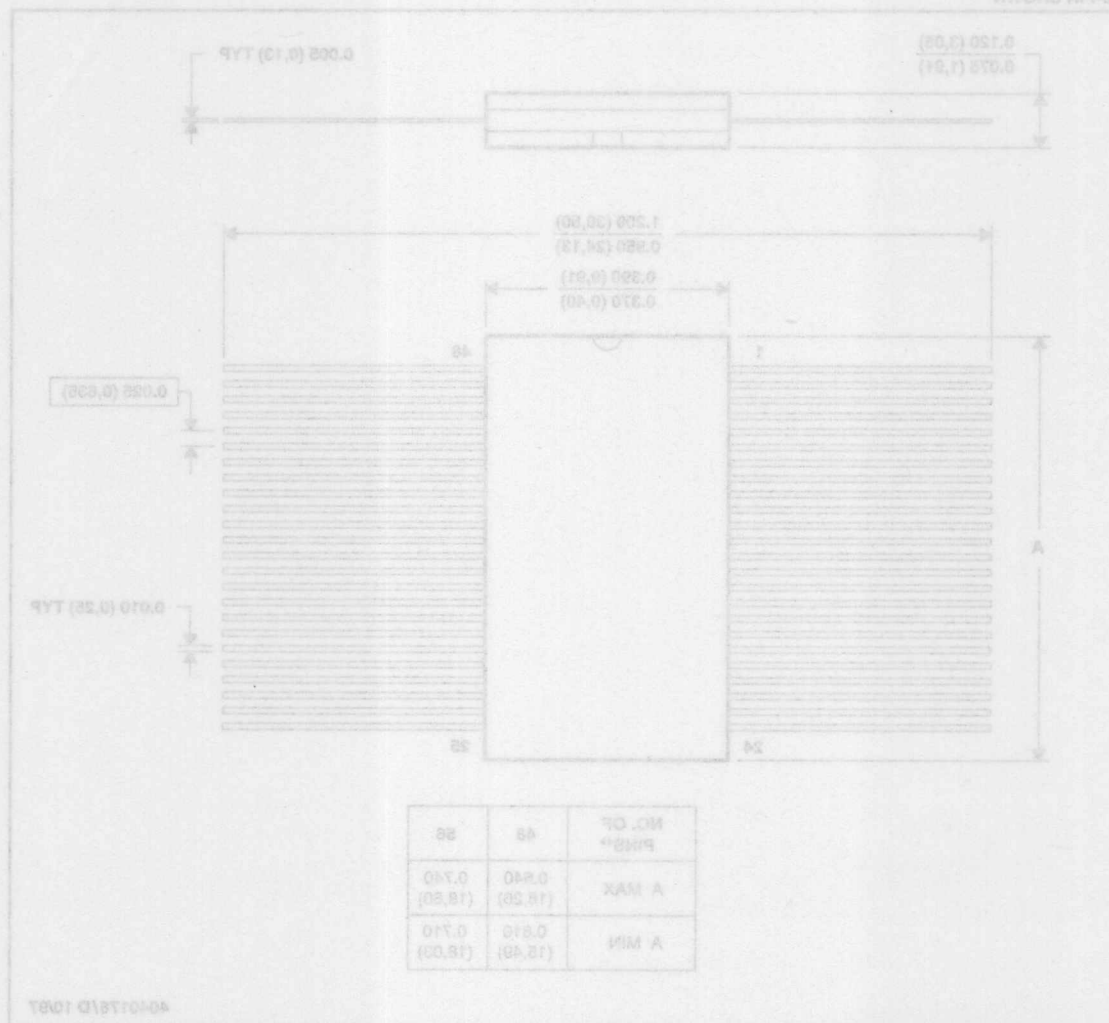


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for pin identification only.
 E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

CERAMIC DUAL FLATPACK

WD (R-GDFF-P)

48-PIN SHOWN



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Lead point is provided on end for pin identification only.
- For MIL-STD-883C: GDFF-P48 and JEDEC MO-168AA.
- For MIL-STD-883C: GDFF-P56 and JEDEC MO-168AB.